DATASHEET

RELEASED 4/20

16Megabit RadTolerant SRAM MCM

UT9Q512K32E

Features

- 25ns maximum (5 Volt supply) address access time
- Asynchronous operation for compatible with industry standard 512K x 8 SRAMs
- TTL compatible inputs and output levels, three-state bidirectional data bus
- Typical radiation performance:
  - Total dose: 100 krads(Si)
  - SEL Immune: 110 MeV-cm^2/mg
  - SEU onset LET$_{th}$: 2.8 MeV-cm^2/mg
  - Saturated Cross Section 2.8E-8 cm^2/bit
    - <1.1E-9 errors/bit-day, Adams 90% worst case environment geosynchronous orbit
- Packaging:
  - 68-lead dual cavity ceramic quad flatpack (CQFP) (11.0 grams)
- Standard Microcircuit Drawing 5962-01511
  - QML Q & V compliant part

Introduction

The UT9Q512K32E RadTol product is a high-performance 2M byte (16Mbit) CMOS static RAM multi-chip module (MCM), organized as four individual 524,288 x 8 bit SRAMs with a common output enable. Memory expansion is provided by an active LOW Chip Enable ($\overline{En}$), an active LOW Output Enable ($\overline{G}$), and three-state drivers. This device has a power-down feature that reduces power consumption by more than 90% when deselected.

Writing to each memory is accomplished by taking Chip Enable ($\overline{En}$) input LOW and Write Enable ($\overline{W}n$) inputs LOW. Data on the eight I/O pins (DQ_0 through DQ_7) is then written into the location specified on the address pins (A_0 through A_{18}). Reading from the device is accomplished by taking Chip Enable ($\overline{En}$) and Output Enable ($\overline{G}$) LOW while forcing Write Enable ($\overline{W}n$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The input/output pins are placed in a high impedance state when the device is deselected ($\overline{En}$ HIGH), the outputs are disabled ($\overline{G}$ HIGH), or during a write operation ($\overline{En}$ LOW and $\overline{W}n$ LOW). Perform 8, 16, 24 or 32 bit accesses by making $\overline{W}n$ along with $\overline{En}$ a common input to any combination of the discrete memory die.

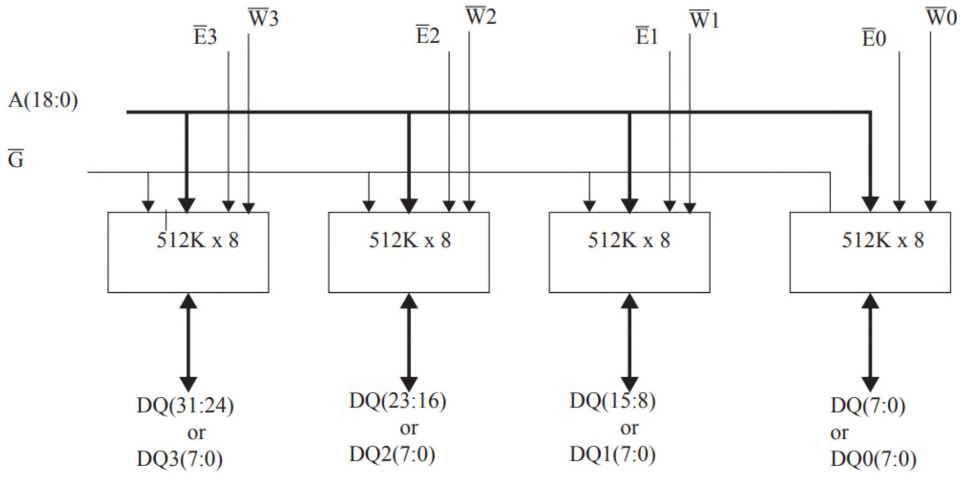

Figure 1. UT9Q512K32E SRAM Block Diagram

UT9Q512K32E

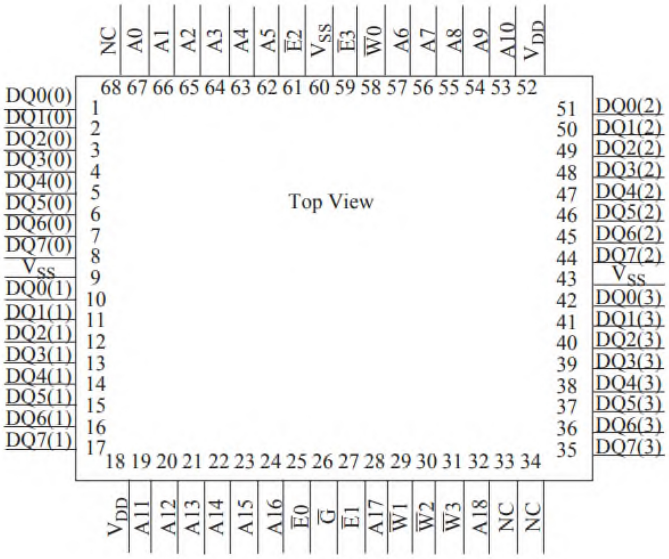

Figure 2. 25ns SRAM Pinout (68)

Pin Names

A(18:0)	Address	$\overline{W}n$	Write Enable
DQn(7:0)	Data Input/Output	$\overline{G}$	Output Enable
$\overline{E}n$	Enable	V_{DD}	Power
		V_{SS}	Ground

Device Operation

The UT9R512K32E has three control inputs called Chip Enable ($\overline{E}n$), Write Enable ($\overline{W}n$), and Output Enable ($\overline{G}$); 19 address inputs, A(18:0); and eight bidirectional data lines, DQ(7:0). $\overline{E}n$ Device Enable controls device selection, active, and standby modes. Asserting $\overline{E}n$ enables the device, causes I_{DD} to rise to its active value, and decodes the 19 address inputs to select one of 524,288 words in the memory. $\overline{W}n$ controls read and write operations. During a read cycle, $\overline{G}$ must be asserted to enable the outputs.

Table 1. Device Operation Truth Table

$\overline{G}$	$\overline{W}n$	$\overline{E}n$	I/O Mode	Mode
X [1]	X	1	3-state	Standby
X	0	0	Data in	Write
1	1	0	3-state	Read [2]
0	1	0	Data out	Read

Notes:

1) "X" is defined as a "don't care" condition.
2) Device active; outputs disabled.

Read Cycle

A combination of $\overline{W}n$ greater than V_{IH} (min) and $\overline{E}n$ less than V_{IL} (max) defines a read cycle. Read access time is measured from the latter of Device Enable, Output Enable, or valid address to valid data output. Read cycles initiate with the assertion of any chip enable or any address change while any chip enable is asserted.

SRAM Read Cycle 1, the Address Access in Figure 4a, is initiated by a change in address inputs while the chip is enabled with $\overline{G}$ asserted and $\overline{W}n$ deasserted. Valid data appears on data outputs DQ(7:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as Device Enable and Output Enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}). Changing addresses prior to satisfying t_{AVAV} minimum results in an invalid operation. Invalid read cycles will require re-initialization.

SRAM Read Cycle 2, the Chip Enable-Controlled Access in Figure 4b, is initiated by $\overline{E}n$ going active while $\overline{G}$ remains asserted, $\overline{W}n$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the eight-bit word addressed by A(18:0) is accessed and appears at the data outputs DQ(7:0).

SRAM Read Cycle 3, the Output Enable-Controlled Access in Figure 4c, is initiated by $\overline{G}$ going active while $\overline{E}n$ is asserted, $\overline{W}n$ is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} have not been satisfied.

Write Cycle

A combination of $\overline{W}n$ less than V_{IL}(max) and $\overline{E}n$ less than V_{IL}(max) defines a write cycle. The state of $\overline{G}$ is a "don't care" for a write cycle. The outputs are placed in the high-impedance state when either $\overline{G}$ is greater than V_{IH}(min), or when $\overline{W}n$ is less than V_{IL}(max).

Write Cycle 1, the Write Enable-Controlled Access in Figure 5a, is defined by a write terminated by $\overline{W}n$ going high, with $\overline{E}n$ still active. The write pulse width is defined by t_{WLWH} when the write is initiated by $\overline{W}n$, and by t_{ETWH} when the write is initiated by $\overline{E}n$. Unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the eight bidirectional pins DQ(7:0) to avoid bus contention.

Write Cycle 2, the Chip Enable-Controlled Access in Figure 5b is defined by a write terminated by $\overline{E}n$ going inactive. The write pulse width is defined by t_{WLEF} when the write is initiated by $\overline{W}n$, and by t_{ETEF} when the write is initiated by the $\overline{E}n$ going active. For the $\overline{W}n$ initiated write, unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the eight bidirectional pins DQ(7:0) to avoid bus contention.

Operational Environment

The UT9Q512K32E SRAM incorporates features which allow operation in a limited environment.

Table 2. Operational Environment Design Specifications [1]

Total Dose	100	krad(Si)
Heavy Ion Error Rate [2]	≤1.1E-9	Errors/Bit-Day
SEL	Immune to 110	MeV-cm^2/mg
SEU Onset LET_{th}	2.8	MeV-cm^2/mg

Notes:

1) The SRAM will not latchup during radiation exposure under recommended operating conditions.
2) 90% worst case particle environment, Geosynchronous orbit, 100 mils of Aluminum.

Absolute Maximum Ratings [1]

(Referenced to V_{SS})

Symbol	Parameter	Limits
V_{DD}	DC supply voltage	-0.5 to 7.0V
$V_{I/O}$	Voltage on any pin	-0.5 to 7.0V
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	1.0W (per byte)
T_J	Maximum junction temperature [2]	+150°C
Θ_{JC}	Thermal resistance, junction-to-case [3]	10°C/W
I_I	DC input current	±10 mA

Notes:

1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2) Maximum junction temperature may be increased to +175°C during burn-in and steady-state life.
3) Test per MIL-STD-883, Method 1012.

Recommended Operating Conditions

Symbol	Parameter	Limits
V_{DD}	Positive supply voltage	4.5 to 5.5V
Tc	Case temperature range	(W) Screen -40 to +105°C
V_{IN}	DC input voltage	0V to V_{DD}

DC Electrical Characteristics (Pre/Post-Radiation) *

-40°C to +105°C (V_{DD} = 5.0V ± 10% for (W) screening)

Symbol	Parameter	Condition		MIN	MAX	Unit
V_{IH}	High-level input voltage	(TTL)		2.0		V
V_{IL}	Low-level input voltage	(TTL)			0.8	V
V_{OL1}	Low-level output voltage	I_{OL} = 8mA, V_{DD} = 4.5V (TTL)			0.4	V
V_{OL2}	Low-level output voltage	I_{OL} = 200µA, V_{DD} = 4.5V (CMOS)			0.08	V
V_{OH1}	High-level output voltage	I_{OH} = -4mA, V_{DD} = 4.5V (TTL)		2.4		V
V_{OH2}	High-level output voltage	I_{OH} = -200µA, V_{DD} = 4.5V (CMOS)		3.0		V
C_{IN1} [1]	Input capacitance; All address and output enable pins	f = 1MHz @ 0V			45	pF
C_{IN2} [1]	Input capacitance; All enable and write enable pins	f = 1MHz @ 0V			18	pF
C_{IO} [1]	Bidirectional I/O capacitance	f = 1MHz @ 0V			25	pF
I_{IN}	Input leakage current	V_{IN} = V_{DD} and V_{SS}, V_{DD} = V_{DD} (max)		-2	2	µA
I_{OZ}	Three-state output leakage current	V_O = V_{DD} and V_{SS} V_{DD} = V_{DD} (max) $\overline{G}$ = V_{DD} (max)		-2	2	µA
I_{OS} [2, 3]	Short-circuit output current	V_{DD} = V_{DD} (max), V_O = V_{DD} V_{DD} = V_{DD} (max), V_O = 0V		-90	90	mA
I_{DD}(OP)	Supply current operating @ 1MHz (per byte)	Inputs: V_{IL} = 0.8V, V_{IH} = 2.0V I_{OUT} = 0mA V_{DD} = V_{DD} (max)			40	mA
I_{DD1}(OP)	Supply current operating @40MHz (per byte)	Inputs: V_{IL} = 0.8V, V_{IH} = 2.0V I_{OUT} = 0mA V_{DD} = V_{DD} (max)			70	mA
I_{DD2}(SB)	Supply current standby @0MHz (per byte)	Inputs: V_{IL} = V_{SS} I_{OUT} = 0mA $\overline{E}$ = V_{DD} - 0.5 V_{DD} = V_{DD} (max) V_{IH} = V_{DD} - 0.5V	-40°C, 25°C		16	mA
			105°C		24	mA

Notes:

*Post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019.

1) Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
2) Supplied as a design limit but not guaranteed or tested.
3) Not more than one output may be shorted at a time for maximum duration of one second.

AC Characteristics Read Cycle (Pre and Post-Radiation)*

-40°C to +105°C (V_{DD} = 5.0V ± 10% for (W) screening)

Symbol	Parameter	MIN	MAX	Unit
t_{AVAV} [1, 6]	Read cycle time	25		ns
$t_{AVS\ K}$ [5]	Address valid to address valid skew time		4	ns
t_{AVQV}	Read access time		25	ns
t_{AXQX} [2]	Output hold time	3		ns
$t_{GLQ\ X}$ [2]	$\overline{G}$-controlled Output Enable time	0		ns
t_{GLQV}	$\overline{G}$-controlled Output Enable time (Read Cycle 3)		10	ns
t_{GHQZ} [2]	$\overline{G}$-controlled output three-state time		10	ns
t_{ETQX} [2, 3]	$\overline{E}$n-controlled Output Enable time	3		ns
t_{AVET2} [5]	Address setup time for read ($\overline{E}$n-controlled)	-4		ns
t_{ETQV} [3]	$\overline{E}$n-controlled access time		25	ns
t_{EFQZ} [1, 2, 4]	$\overline{E}$n-controlled output three-state time		10	ns

Notes:

*Post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019.

1) Functional test.
2) Three-state is defined as a 500mV change from steady-state output voltage.
3) The ET (chip enable true) notation refers to the latter falling edge of $\overline{E}$n. SEU immunity does not affect the read parameters.
4) The EF (chip enable false) notation refers to the latter rising edge of $\overline{E}$n. SEU immunity does not affect the read parameters.
5) Guaranteed by design
6) Address changes prior to satisfying t_{AVAV} minimum is an invalid operation

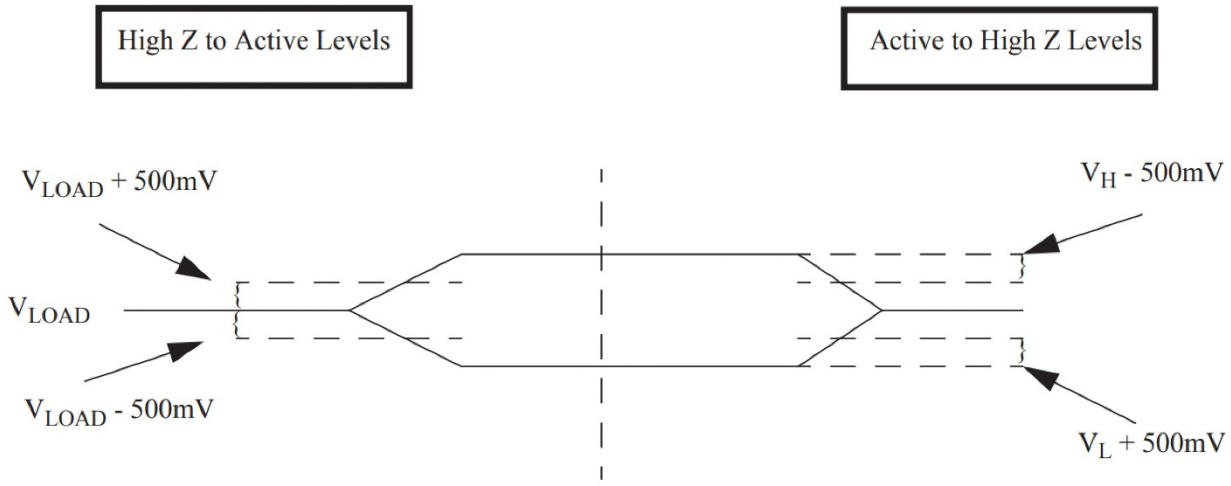

Figure 3. 5-Volt SRAM Loading

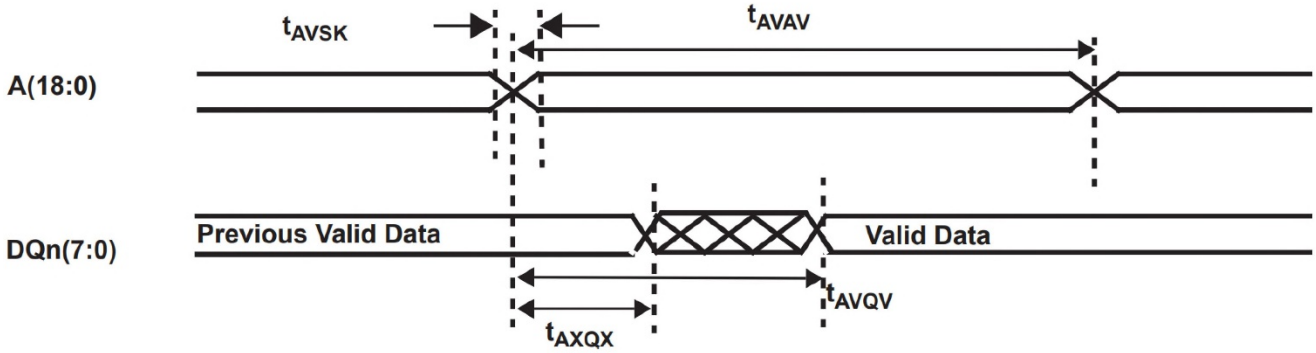

Figure 4a. SRAM Read Cycle 1: Address Access

Assumptions:

1) $\overline{E}n$ and $\overline{G} \leq V_{IL}$(max) and $\overline{W}n \geq V_{IH}$(min)

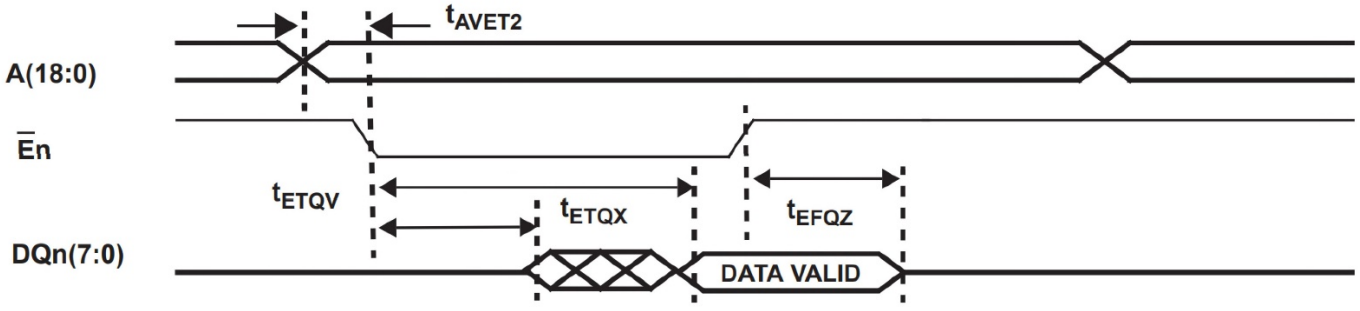

Figure 4b. SRAM Read Cycle 2: Chip Enable-Controlled Access

Assumptions:

1) $\overline{G} \leq V_{IL}$ (max) and $\overline{W}n \geq V_{IH}$ (min)

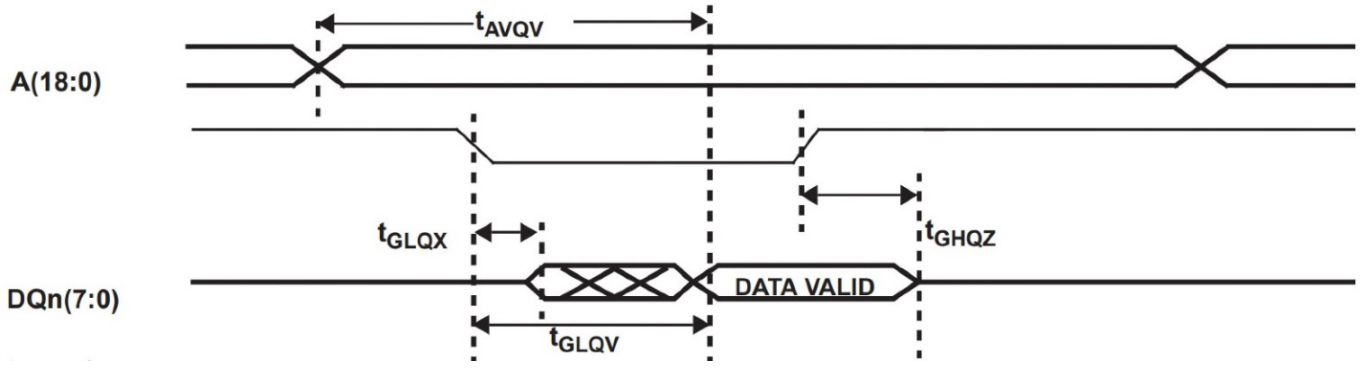

Figure 4c. SRAM Read Cycle 3: Output Enable-Controlled Access

Assumptions:

1) $\overline{E}n \leq V_{IL}$ (max) and $\overline{W}n \geq V_{IH}$(min)

AC Characteristics Write Cycle (Pre/Post-Radiation)*

-40°C to +105°C (V_{DD} = 5.0V ± 10% for (W) screening)

Symbol	Parameter	MIN	MAX	Unit
t_{AVAV} [1]	Write cycle time	25		ns
t_{ETWH}	Device Enable to end of write	20		ns
t_{AVET}	Address setup time for write ($\overline{E}n$ - controlled)	1		ns
t_{AVWL}	Address setup time for write ($\overline{W}n$ - controlled)	0		ns
t_{WLWH}	Write pulse width	20		ns
t_{WHAX}	Address hold time for write ($\overline{W}n$ - controlled)	0		ns
t_{EFAX}	Address hold time for Device Enable ($\overline{E}n$ - controlled)	0		ns
t_{WLQZ} [2]	$\overline{W}n$ - controlled three-state time		10	ns
t_{WHQX} [2]	$\overline{W}n$ - controlled Output Enable time	5		ns
t_{ETEF}	Device Enable pulse width ($\overline{E}n$ - controlled)	20		ns
t_{DVWH}	Data setup time	15		ns
t_{WHDX}	Data hold time	2		ns
t_{WLEF}	Device Enable controlled write pulse width	20		ns
t_{DVEF}	Data setup time	15		ns
t_{EFDX}	Data hold time	2		ns
t_{AVWH}	Address valid to end of write	20		ns
t_{WHWL} [1]	Write disable time	5		ns

Notes:

*Post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019

1) Functional test performed with outputs disabled ($\overline{G}$ high).
2) Three-state is defined as 500mV change from steady-state output voltage (see Figure 3).

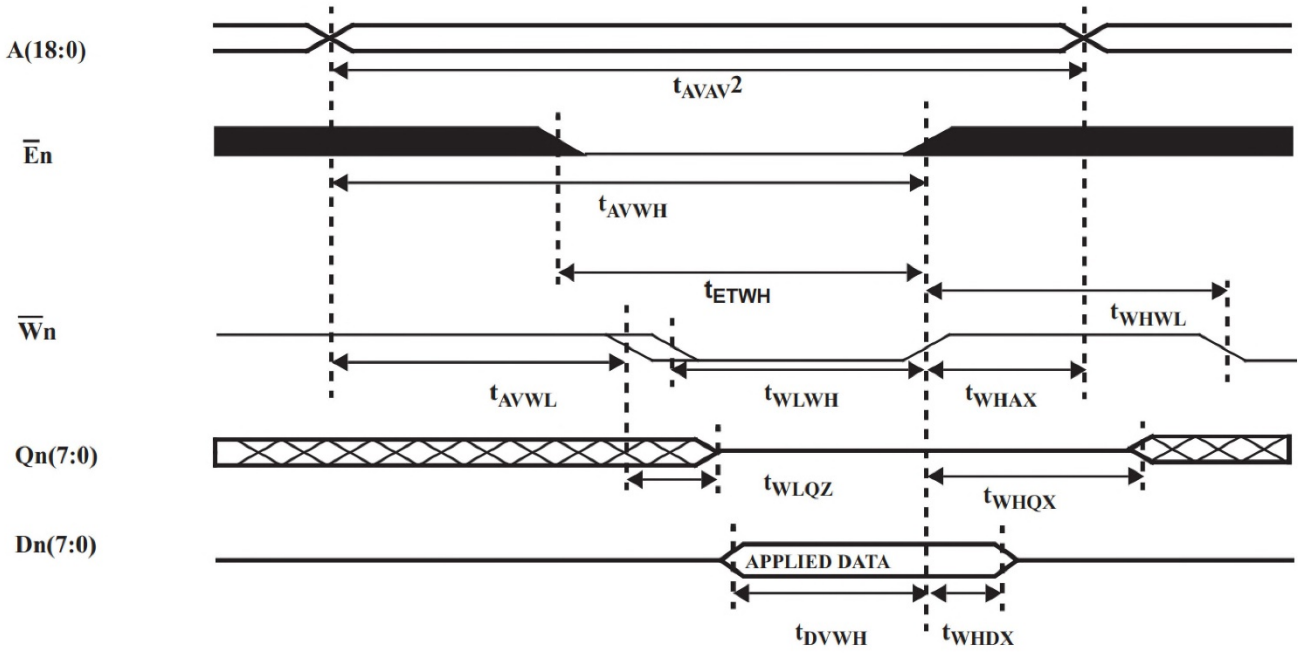

Figure 5a. SRAM Write Cycle 1: Write Enable – Controlled Access

Assumptions:

1) $\overline{G} \leq V_{IL}$ (max). If $\overline{G} \geq V_{IH}$ (min) then Qn(7:0) will be in three-state for the entire cycle.
2) $\overline{G}$ high for t_{AVAV} cycle.

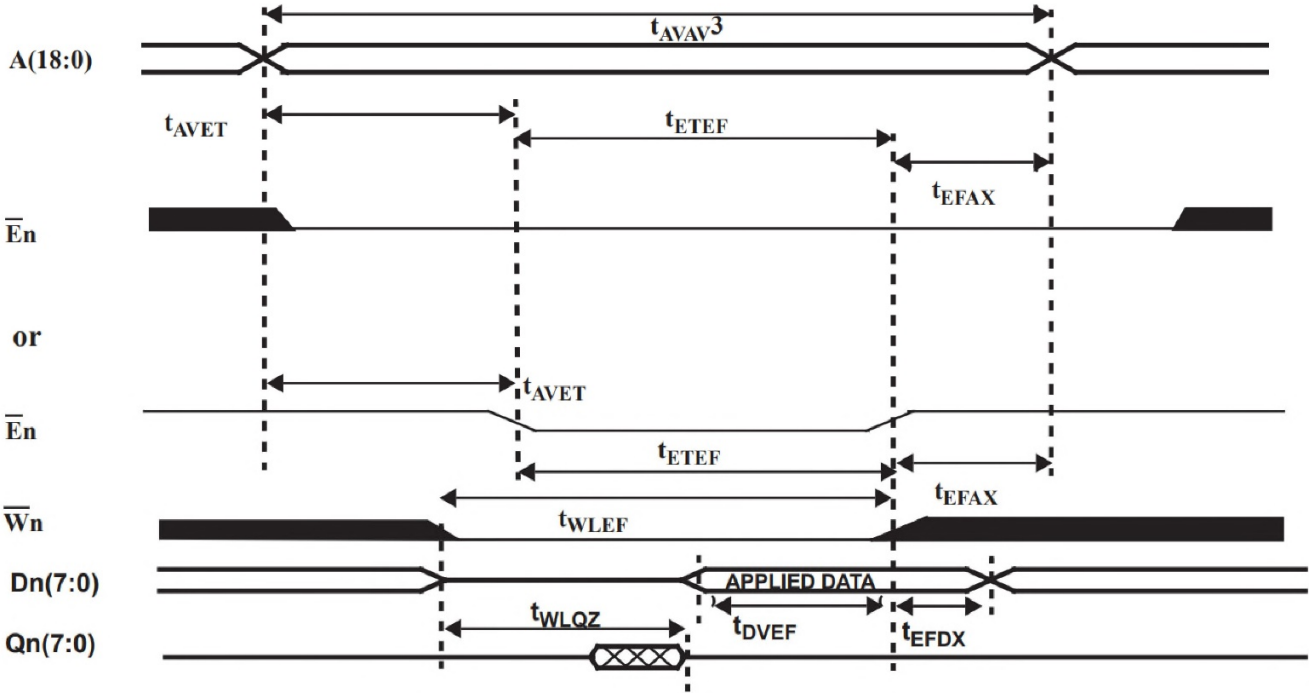

Figure 5b. SRAM Write Cycle 2: Chip Enable - Controlled Access

Assumptions & Notes:

1) $\overline{G} \leq V_{IL}$ (max). If $\overline{G} \geq V_{IH}$ (min) then Qn(7:0) will be in three-state for the entire cycle.
2) Either $\overline{E}n$ Scenario above can occur.
3) $\overline{G}$ high for t_{AVAV} cycle.

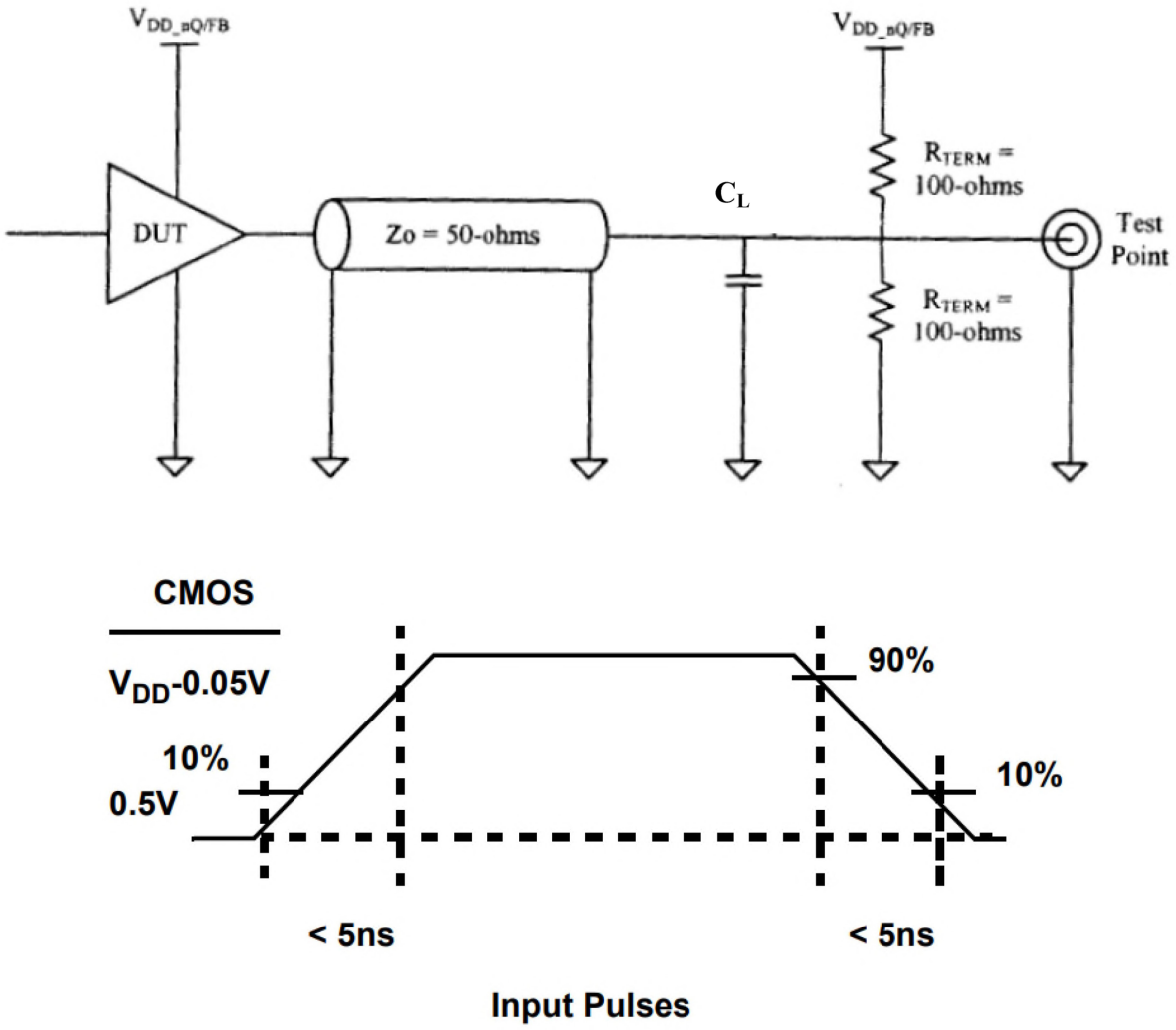

Figure 6. AC Test Loads and Input Waveforms

Notes:

1) 50pF including scope probe and test socket capacitance.
2) Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input = $V_{DD}/2$).

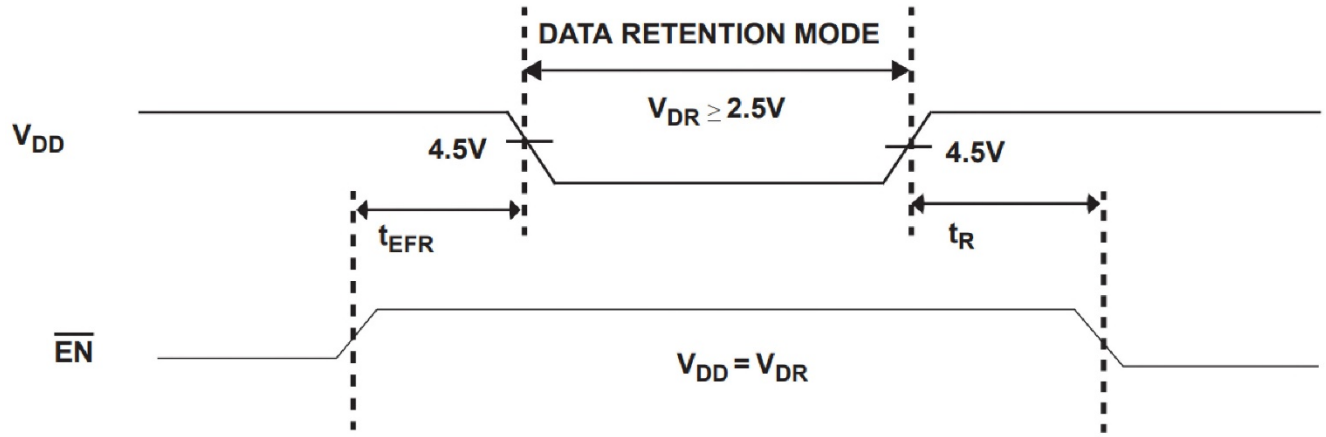

Figure 7. Low V_{DD} Data Retention Waveform

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Data Retention Characteristics (Pre-Radiation)*

(V_{DD} = V_{DD} (min), 1 Sec DR Pulse)

Symbol	Parameter	TEMP	Minimum	Maximum	Unit
V_{DR}	V_{DD} for data retention	--	2.5	--	V
I_{DDR} [1]	Data retention current (per byte)	-40°C	--	16	mA
		25°C	--	16	mA
		105°C	--	24	mA
t_{EFR} [1,2]	Chip deselect to data retention time	--	0	--	ns
t_R [1,2]	Operation recovery time	--	t_{AVAV}	--	ns

Notes:

*Post-radiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019.

1) $\overline{E}n$ = V_{DR} all other inputs = V_{DR} or V_{SS}.
2) Not guaranteed or tested

Packaging

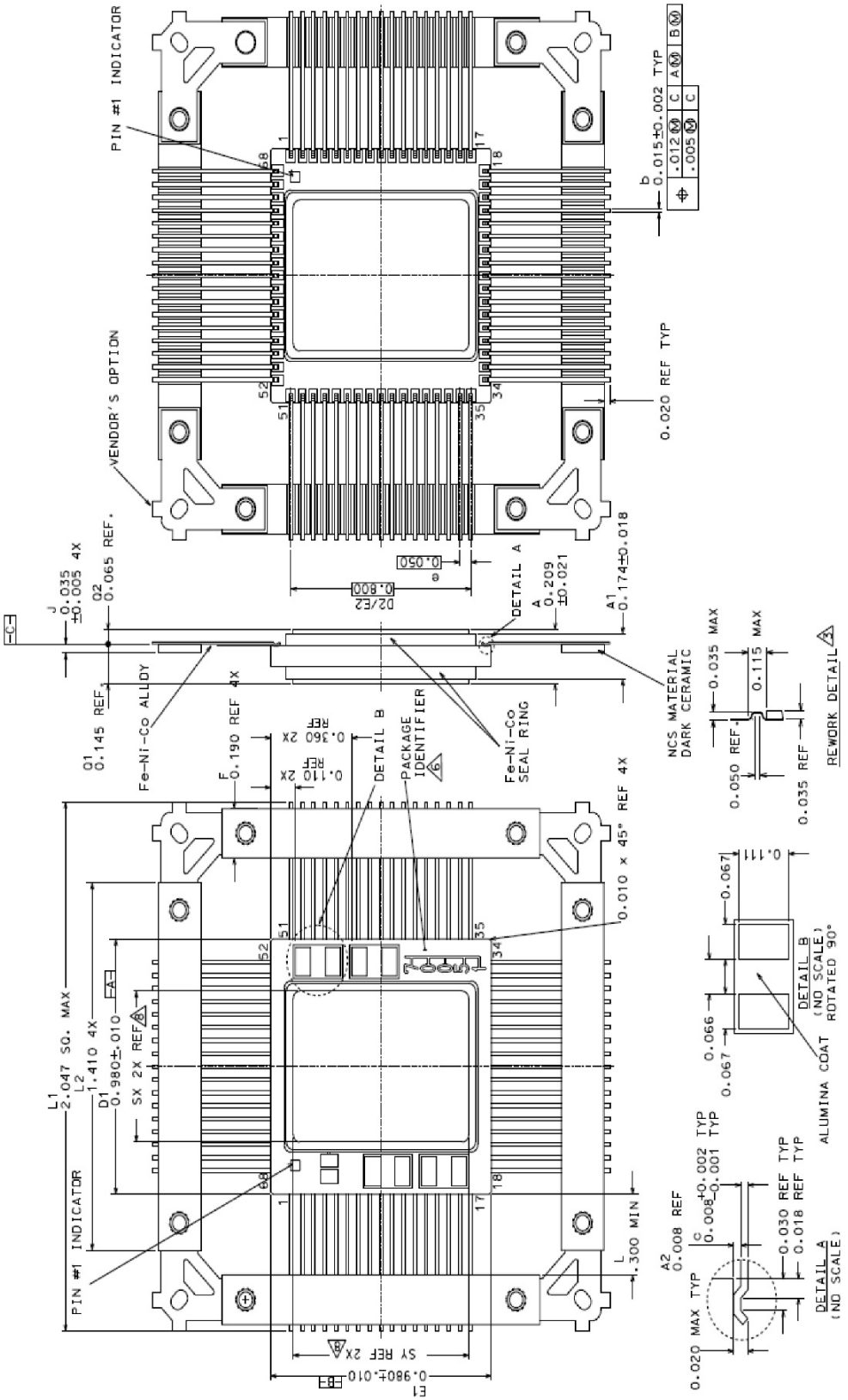


Figure 8. 68-Lead Ceramic Quad Flatpack

Notes:

1) All exposed metalized areas are gold plated over nickel plating per MIL-PRF-38535.
2) Both Lids are electrically connected to VSS.
3) Packages may be shipped with repaired leads as shown.
4) Coplanarity requirements do not apply in repaired area.
5) Letter designations are to cross reference to MIL-STD-1835.
6) Lead true position tolerances and coplanarity are not measured.
7) Capacitor pads are sized to fit CDR32 (1206) capacitors.
8) Package can be solder or seam sealed. The table below provides Dimensions for these Lid types:

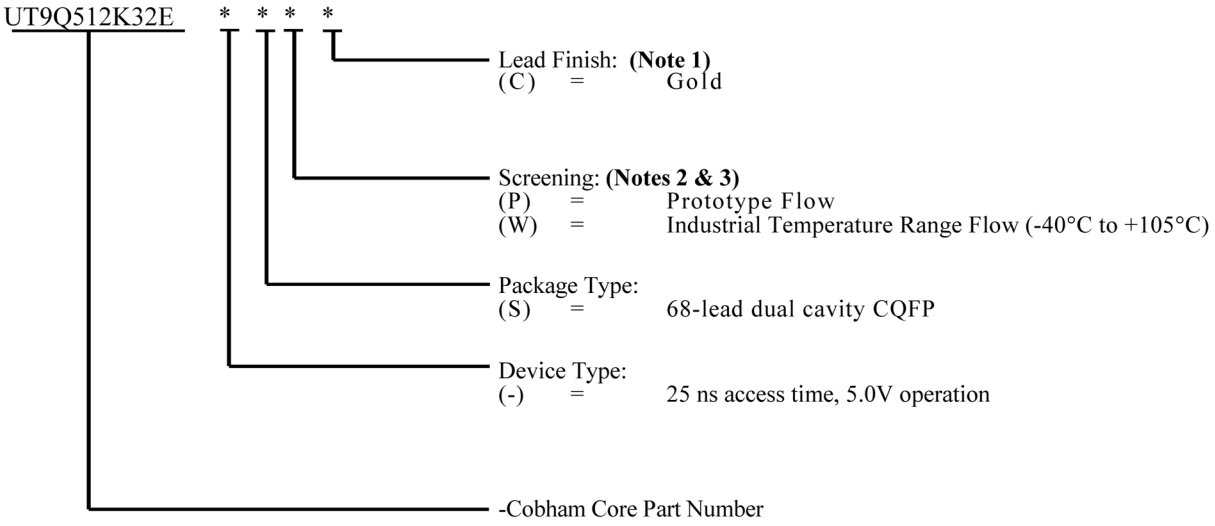
Seal Type	SX	SY
Solder Seal	0.580	0.780
Seam Seal	0.638	0.840

16Megabit RadTolerant SRAM MCM

UT9Q512K32E

Ordering Information

512K32E 16Megabit SRAM MCM:



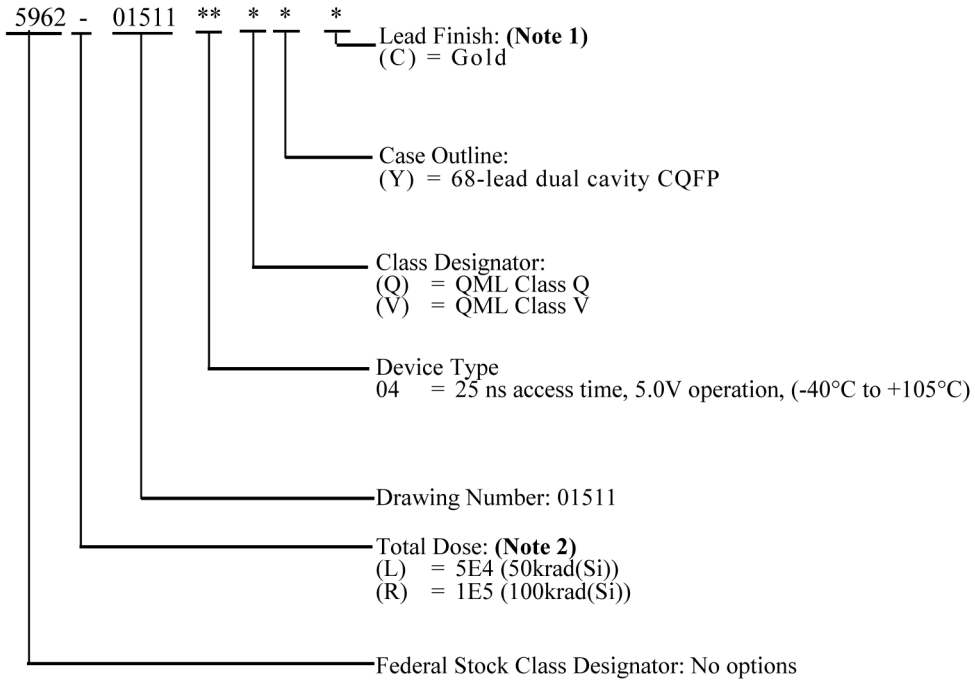
Notes:

1) Gold lead finish only.
2) Prototype flow per CAES Colorado Springs Manufacturing Flows Document. Tested at 25°C only. Radiation neither tested nor guaranteed.
3) Extended Industrial Range flow per CAES Colorado Springs Manufacturing Flows Document. Devices are tested at -40°C to 105°C. Radiation neither tested nor guaranteed.

16Megabit RadTolerant SRAM MCM

UT9Q512K32E

512K32E 16 Megabit SRAM MCM: SMD



Notes:

1) Lead finish is "C" (Gold) only.
2) Total dose radiation must be specified when ordering.

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Revision History

Date	Revision	Change Description
July 15, 2019	A	Changed template to CAES
April 2020	B	Raised max TID to 100krads (Si); Typo fixes; Split input capacitance to clarify capacitance differences between bussed inputs and single inputs; Increased standby current to 16mA; added note to data retention table (pg 12); change package identification marking on package outline; revised SMD PN buildup page to reflect new device type and TID offering; corrected error in test load figure 6

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16Megabit RadTolerant SRAM MCM

UT9Q512K32E

Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

The following United States (U.S.) Department of Commerce statement shall be applicable if these commodities, technology, or software are exported from the U.S.: These commodities, technology, or software were exported from the United States in accordance with the Export Administration Regulations. Diversion contrary to U.S. law is prohibited.