AEROSPACE DATA EXCHANGE PROGRAM TRANSMITTAL

PROBLEM ADVISORY

CAES

1. TITLE UT699 LEON3FT PROCESSOR CACHE CONTROLLER: INSTRUCTION CACHEING ERROR DUE TO HCACHE TIMING	**2. DOCUMENT NUMBER** SPO-2014-PA-0005
	3. DATE *(Year, Month, Date)* 2014, August, 29
4. MANUFACTURER NAME AND ADDRESS CAES 4350 CENTENNIAL BOULEVARD COLORADO SPRINGS, COLORADO 80907-3486	**5. MANUFACTURER POINT OF CONTACT NAME** Peter Pohlenz
	6. MANUFACTURER POINT OF CONTACT TELEPHONE (719) 594-8000
	7. MANUFACTURER POINT OF CONTACT EMAIL Peter.Pohlenz@cobhamaes.com

8. CAGE CODE	9. LDC START	10. LDC END	11. PRODUCT IDENTIFICATION CODE	12. BASE PART
65342	All	All	WG07A	UT699

13. BLANK	14. SMD NUMBER	15. DEVICE TYPE DESIGNATOR
	5962-08228	ALL
	16. RHA LEVELS	**17. QML LEVEL**
	ALL	ALL
	18. NON QML LEVEL	**19. BLANK**
	ALL	

20. PROBLEM DESCRIPTION / DISCUSSION / EFFECT

This document discusses an errata in GRLIB IP (rev. 1.0.22-b4101 and previous) based devices, when used together with a memory controller that drives the HCACHE AMBA side-band signal with a nonconstant value to signal cacheability of different memory areas.

Refer to SHEET 2 for list of affected parts.

When an instruction is fetched immediately after an access to the memory controller's memory-mapped IO area it will not set its valid bit when written into the instruction cache. This occurs because the AMBA side-band signal HCACHE, generated by the memory controller, changes one cycle too late in this situation. This results in the instruction being fetched again the next time it is excecuted. The fetched instruction will execute correctly, the impact is on execution timing only.

ACTION TAKEN / PLANNED

1. Create an errata to describe the workaround and mitigation methods to handle the error. (Complete – LEON Processor Cache Controller Errata: Instruction treated as noncacheable due to HCACHE timing i1r2 – appended to this Problem Advisory, please contact support@gaisler.com for updates to errata)
2. The errata will be corrected in the next LEON3FT (Vendor Generic P.N. UT699E / SMD 5962-13237). (Prototypes available NOW / QML target availability 3QCY14) The revised UT699E is only offered in a 484 Ceramic Land Grid Array, Ceramic Ball Grid Array and Ceramic Column Grid Array

21. DISPOSITIONARY RECOMMENDATION:	CHECK & USE AS IS ☒	CONTACT MANUFACTURER ☐	REMOVE & REPLACE ☐	CORRECT & USE AS SPECIFIED ☐

22. ADEPT REPRESENTATIVE	23. SIGNATURE	24. DATE
Timothy L. Meade	Timothy L. Meade	**August 29, 2014**

SHEET 2

Affected Parts

UT699-ZPC	5962F0822801QXC	LEON3FT-RTAX-IC1
UT699-SPA	5962R0822801QXC	LEON3FT-RTAX-IC2
UT699-CPA	5962F0822802QXC	LEON3FT-RTAX-SC1
UT699-XPC	5962R0822802QXC	LEON3FT-RTAX-SC2
UT699-XEC	5962F0822801VXC	LEON3FT-RTAX-SC3
UT699-ZEC	5962R0822801VXC	LEON3FT-RTAX-SC4
UT699-SEA	5962F0822801QYC	LEON3FT-RTAX-PC1
UT699-CEA	5962R0822801QYC	LEON3FT-RTAX-PC2
	5962F0822802QYC	
	5962R0822802QYC	
	5962F0822801VYC	
	5962R0822801VYC	
	5962F0822801QZA	
	5962R0822801QZA	
	5962F0822802QZA	
	5962R0822802QZA	
	5962F0822801VZA	
	5962R0822801VZA	
	5962R0822803QXC	
	5962R0822803QYC	
	5962R0822803QZA	
	5962R0822803VXC	
	5962R0822803VYC	
	5962R0822803VZA	

LEON Processor Cache Controller Errata: Instruction treated as noncacheable due to HCACHE timing

1 OVERVIEW

This document describes a design errata in certain versions of the LEON3 and LEON3FT processors when used together with a memory controller that drives the HCACHE AMBA side-band signal with a nonconstant value to signal cacheability of different memory areas. The impact of the error, which versions are affected, and possible workarounds are described.

For further information, contact CAES Gaisler support: support@gaisler.com

2 AFFECTED PRODUCTS

2.1 General

This errata applies to some LEON3/LEON3FT-based devices made using GRLIB revisions earlier than revision b4101.

2.2 CAES components

CAES components/products affected are:

- UT699
- LEON3FT-RTAX Subset of devices affected, contact CAES Gaisler Support

CAES components **NOT** affected are:

- GR712RC NOT affected, processor configuration immune from errata
- UT699E NOT affected, made from a newer revision of GRLIB
- UT700 NOT affected, made from a newer revision of GRLIB
- LEON4-N2X NOT affected, made from a newer revision of GRLIB

2.3 How to check if a design is affected

If you are licensing GRLIB for use in your own FPGA or ASIC design, you can check the following conditions in the design's VHDL source to see if the erratum applies to your system:

1. Check the GRLIB revision. This can be seen in the file name of the downloaded release package, in the directory name after unpacking the release, and in the file lib/grlib/stdlib/version.vhd in the release file tree (constant grlib_build). If this is higher than 4101, you are NOT affected by this error. Otherwise, continue with the following step.

2. Check if you are using a memory controller that toggles the HCACHE AMBA sideband signal. This is the case for most memory controllers in GRLIB that supports a memory-mapped IO area, such as MCTRL and FTMCTRL. If you have a memory controller that drives a constant value on the HCACHE output then you are NOT affected by this error. Otherwise continue with the following step.

3. Check the configuration of the VHDL generic *cached* on the LEON3 processor

    - Designs with GRLIB build ID 2694 are affected by the bug

    - Designs with GRLIB build ID 2695 – 4100 where the *cached* VHDL generic is 0 are affected by the bug.

    - Designs with GRLIB build ID 2695 – 4100 where the *cached* VHDL generic is nonzero are NOT affected by the bug.

3 IMPACT

On systems where the errata is applicable and not using any of the workarounds described in this document, the impact is suboptimal behaviour of the instruction cache in the case of back-to-back fetch after an IO area access. When an instruction is fetched back-to-back with an access to the memory controller's memory-mapped IO area, it will not get its valid bit set when written into the instruction cache and will therefore be fetched again the next time it is executed. The fetched instruction will still be executed correctly, so the impact is on execution timing only.

The errata does not affect applications where the uncacheable (memory-mapped I/O) area of the memory controller is never accessed. An upper bound on the impact is one extra instruction cache miss per performed IO area read or write. This errata is primarily a concern for applications doing a large number of memory-mapped I/O reads or writes in a loop where the loop code may not become properly cached and therefore execute slower than expected.

4 ERRATA DESCRIPTION

The underlying reason for the problem is that the AMBA side-band signal HCACHE generated by the memory controller changes one cycle too late when you perform a PROM/SRAM/SDRAM access (where the memory controller drives HCACHE=1) back-to-back after an IO access (where the memory controller drives HCACHE=0). This makes the LEON3 instruction cache not write in the first word into cache.

This only affects instruction fetches and not data fetches, because for design reasons the processor does not use the HCACHE signal for data fetches (it uses the static AMBA plug'n'play information instead). The only impact of this bug that has been identified is that an instruction fetch immediately after an access to an I/O area will not be stored in cache. The instruction will still be executed correctly, the impact is timing only.

5 SOLUTIONS

5.1 Workaround: Dry-run

One software workaround for the problem is to perform a dry-run through any code that accesses the memory-mapped IO area of the memory controller. During the first run of the code, the read/write access should be performed to a cacheable area, such as the SRAM area, to ensure that this errata does not trigger and any fetched instructions are written correctly into the instruction cache. The pointer to the SRAM area is then swapped with the pointer to the IO area and the same instructions are re-run from cache, avoiding the back-to-back code fetch.

5.2 VHDL correction

If you have access to the RTL sources of the design then the timing of the HCACHE signal can be corrected. Please contact CAES Gaisler support for additional details.