

PROBLEM ADVISORY

1. TITLE UT700 LEON3 FT SPARC V8 Microprocessor, 1553 peripheral transmission glitches on power-up sequence			2. DOCUMENT NUMBER SPO-2021-PA-0003									
			3. DATE (Year, Month, Date) 2021, February 1st									
4. MANUFACTURER NAME AND ADDRESS CAES 4350 CENTENNIAL BOULEVARD COLORADO SPRINGS, COLORADO 80907-3486			5. MANUFACTURER POINT OF CONTACT NAME info-hirel@cobhamaes.com									
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8. CAGE CODE 65342	9. LDC START All	10. LDC END All	11. PRODUCT IDENTIFICATION CODE See table below	12. BASE PART See table below								
13. BLANK			14. SMD NUMBER See table below	15. DEVICE TYPE DESIGNATOR 01								
			16. RHA LEVELS R	17. QML LEVEL See table below								
			18. NON QML LEVEL N/A	19. GIDEP NUMBER GB4-P-21-03								
20. PROBLEM DESCRIPTION / DISCUSSION / EFFECT This document describes a corner case that affects all versions of the UT700 LEON 3FT SPARC V8 Microprocessor. (see appended).												
<table border="1"> <thead> <tr> <th>Base part number</th> <th>PIC</th> <th>SMD number</th> <th>QML Level</th> </tr> </thead> <tbody> <tr> <td>UT700</td> <td>WQ03</td> <td>5962-13238</td> <td>Q, V</td> </tr> </tbody> </table>					Base part number	PIC	SMD number	QML Level	UT700	WQ03	5962-13238	Q, V
Base part number	PIC	SMD number	QML Level									
UT700	WQ03	5962-13238	Q, V									
21. ACTION TAKEN / PLANNED Please see appended description for all versions of the UT700 LEON 3FT SPARC V8 Microprocessor.												
22. DISPOSITIONARY RECOMMENDATION:	CHECK & USE AS IS <input type="checkbox"/>	CONTACT MANUFACTURER <input type="checkbox"/>	REMOVE & REPLACE <input type="checkbox"/>	CORRECT & USE AS SPECIFIED <input type="checkbox"/>								

Description

When the LEON processor is powering up with a minimum core voltage setting, its embedded 1553 module transmission signals might glitch (see Figure 1).

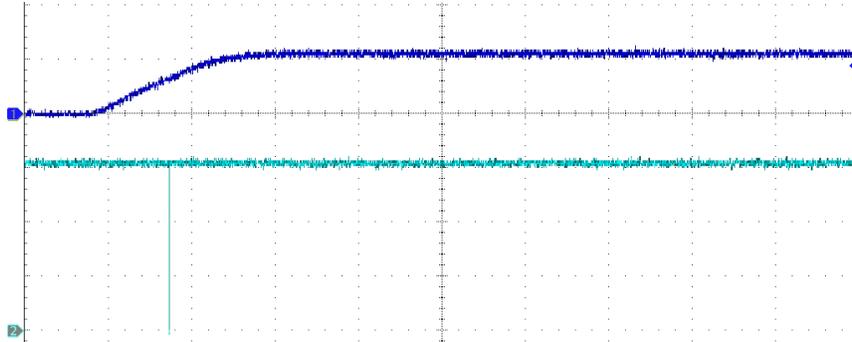


Figure 1: The figure shows the core voltage (blue color) during the powering up sequence and a glitch on the 1553 transmission signal (cyan color).

Impact

This anomaly will not affect the functionality of the 1553 module, but the transmission signal glitches might interrupt an active 1553 network operation.

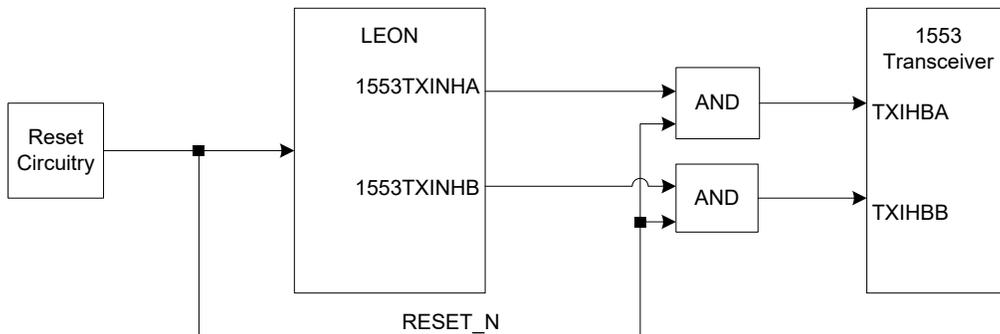


Figure 2: This workaround prevents power up sequence glitches from getting out to the 1553 network

Workaround

A simple circuitry can mitigate this anomaly by using the external reset signal to gate the 1553TXINHA and 1553TXINHB, driving the TXIHA and TXIHB signals on the 1553 transceiver. This configuration (see Figure 2), gating the RESET_N with 1553TXINHA/B, blocks the glitched signals from propagating onto the 1553 bus.

Additional Reference

Refer to the **RT-Validation Result Clarifications Memorandum** for additional configuration requirements for the LEON 1553 module.