FRONTGRADE

Xilinx Kintex Ultrascale KU060 Ecosystem Design Examples

January 2025

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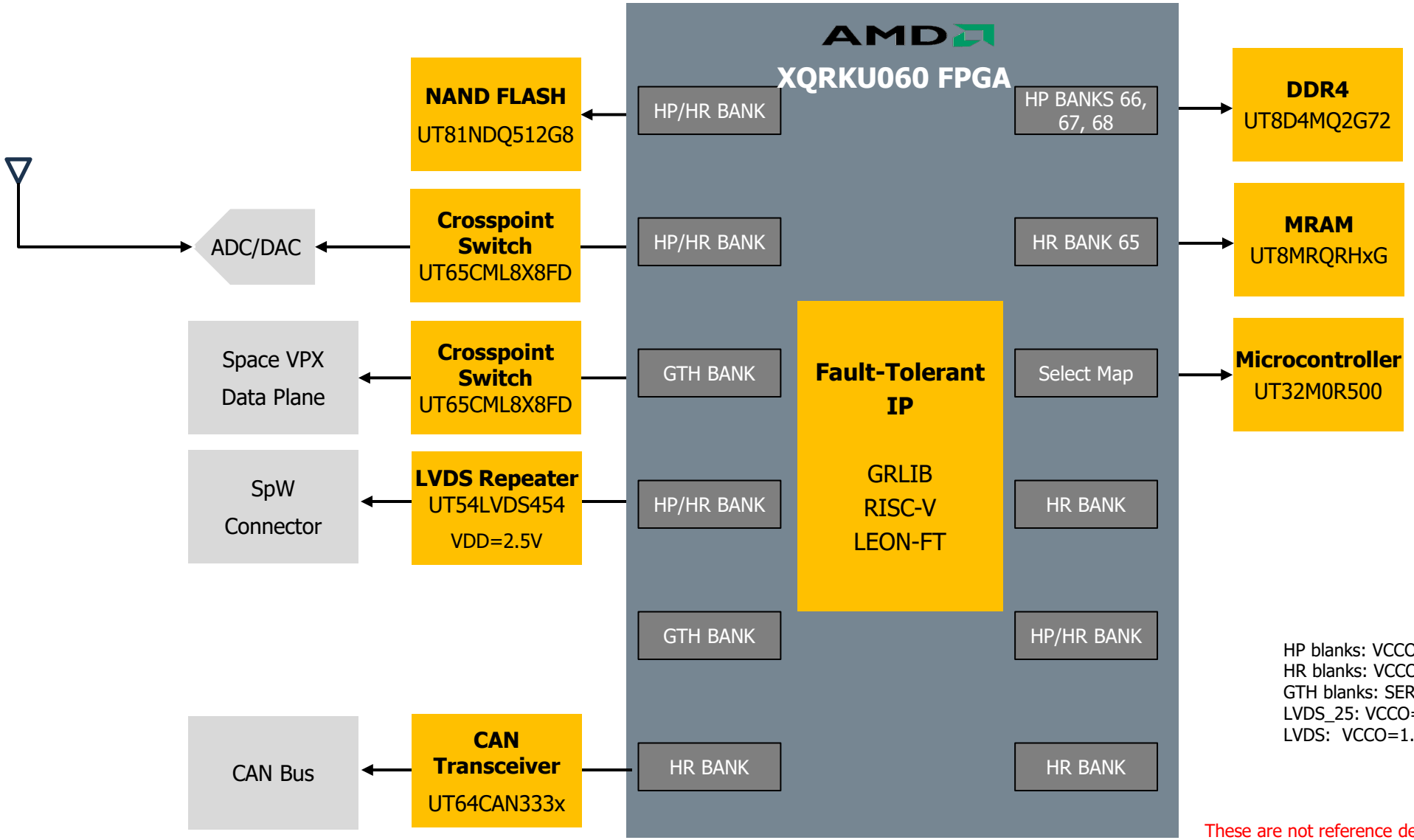
Frontgrade KU060 FPGA Ecosystem



HP blanks: VCCO=1.0V-1.8V
HR blanks: VCCO=1.2V-3.3V
GTH blanks: SERDES (Gbps)
LVDS_25: VCCO=2.5V (HR)
LVDS: VCCO=1.8V (HP)

These are not reference designs. They are conceptual approaches for guidance purposes only.
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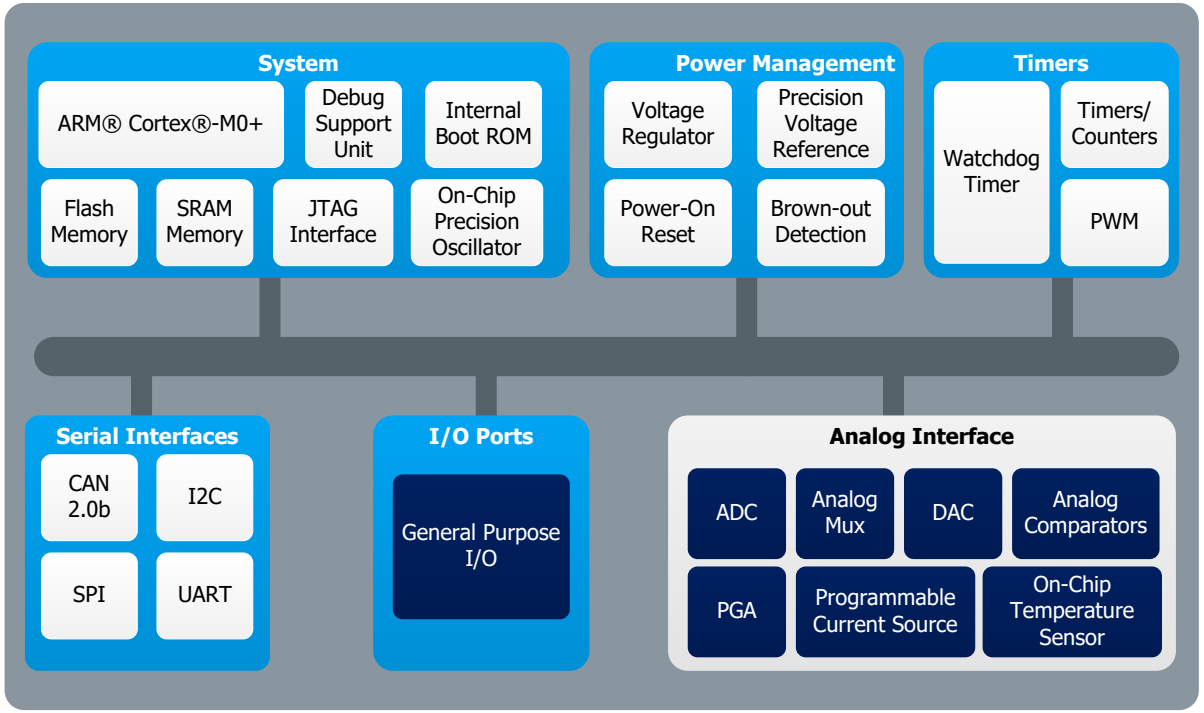
UT32M0R500 Microcontroller

KU060 – UT32M0R500

32-bit Arm® Cortex®-M0+ Microcontroller

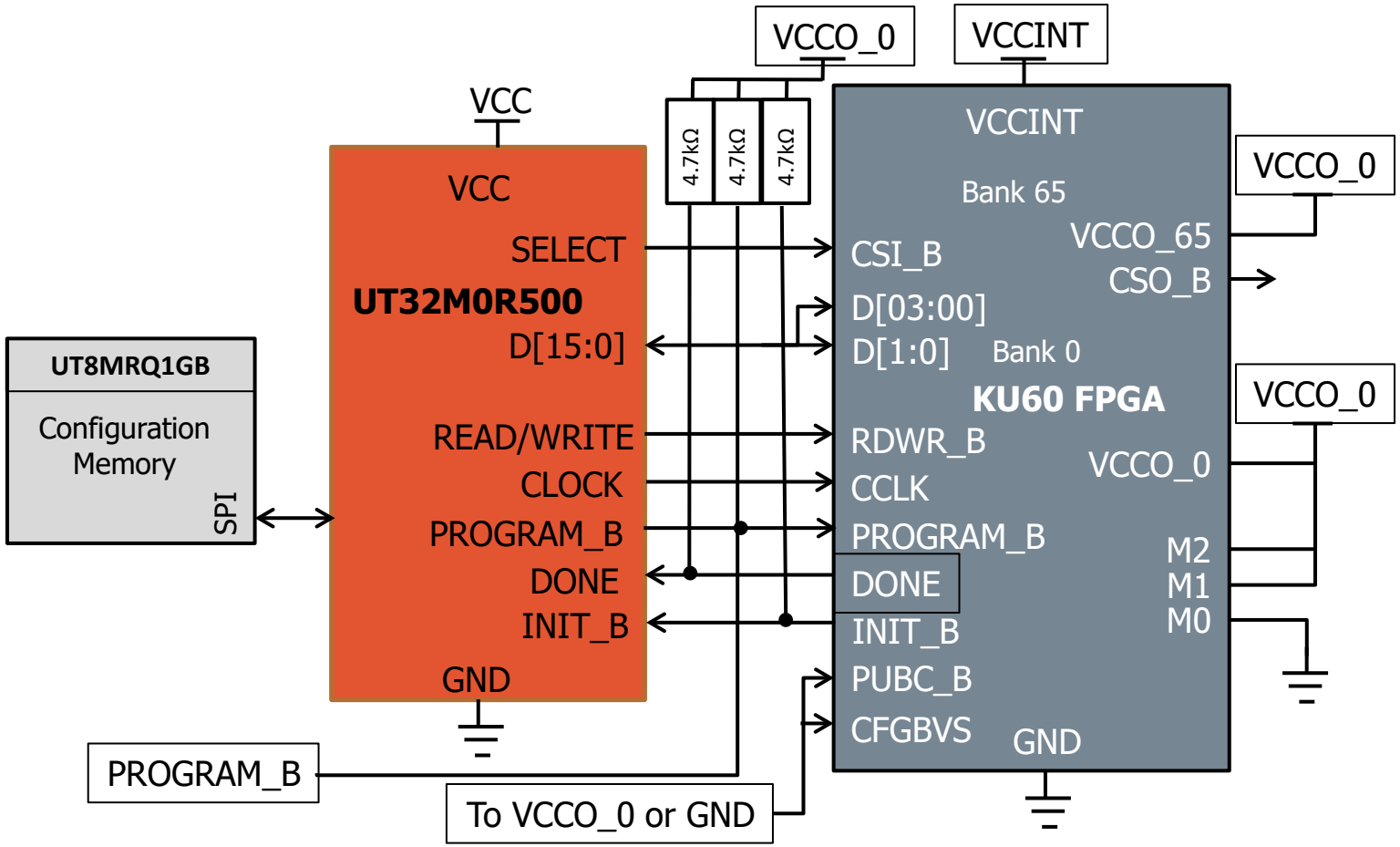


Part Number	UT32M0R500
SMD#	5962-17212
Processor	32-bit ARM® Cortex®-M0+ @ 50MHz
Memory	96KB dual port SRAM w/ EDAC + scrubber
	64Mb Flash (integrated)
Supply Voltage	+3.3V
Analog	• 12-bit ADC w/ PGA and Mux • Precision Current Source • Two DACs • Two Comparators • Timers • PWMs
Interfaces	• Two CAN 2.0B • 2x I2C, 2x SPI, 48x GPIO, 2x UART, JTAG, WDT
Process Technology	130nm TSMC
Typical Power	300mW
Package	143 pin CLGA, CBGA, CCGA options 14.5 x 14.5mm, 1mm pitch
Operational Environment	
Temp Range:	-55°C to 105°C
TID:	50 Krad (Si)
SEL Immune:	LET <= 80 MeV-cm²/mg @105°C
Qualifications	QML-Q, Q+ and Constellation Grade

Development Support

- Keil development tool environment
- API library with source code examples
- UT32M0R500-EVB dev. board

KU060 – UT32M0R500 SelectMAP Interface



Interface:

- UT32M0R500 - UT8MRQ1GB
  - UT32M0R500 operates SPI bus
- UT32M0R500 - KU060
  - KU060 SelectMAP pins to UT32M0R500 GPIO pins, 16-bit wide data
  - KU060 control signals connected to UT32M0R500 GPIO pins

Operation:

- UT8MRQ1GB (Frontgrade 1Gb SPI MRAM) stores up to four KU060 configuration images
- UT32M0R500 performs initial configuration of KU060
  - Reads a configuration image from the UT8MRQ1GB, writes to the KU060 via the SelectMAP interface UT8MRQ1GB
- UT32M0R500 performs blind scrubbing on KU060
  - Regularly refreshes KU060 configuration memory with configuration data from the UT8MRQ1GB

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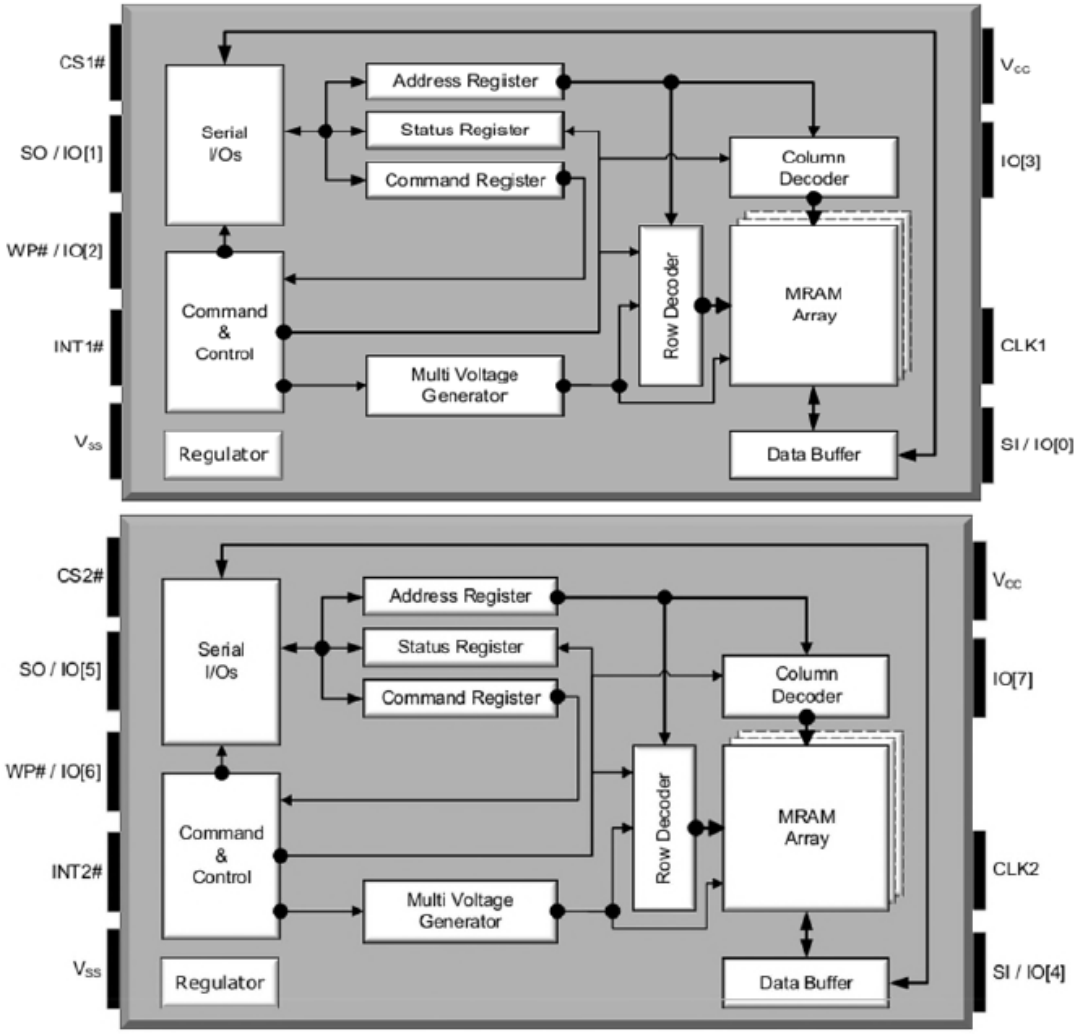
UT8MRQRHxG MRAM Memory

MRAM Memory
Product Details

Functional Block Diagram
(Dual Quad SPI Interface)



Part Number	UT8MRQRHxG
Density	1,2,4,8 Gb
Interface	SPI
Configuration	2x Quad
Supply Voltage	+3.3V core; 1.8, 2.5V, 3.3V IO supplies
Write Endurance	10^{16} write cycles
Data Retention	> 10 years @ 85°C
Process Technology	22nm pMTJ STT
Temp Range	-40°C to +125°C
Package	224-ball FBGA (20x20 mm)
Operational Environment	
TID:	100 krad (Si)
SEL:	78 MeV-cm^2/mg @105°C, 2.7V
Qualifications	PEM L2, L1

UT8MRQRHxG MRAM Memory

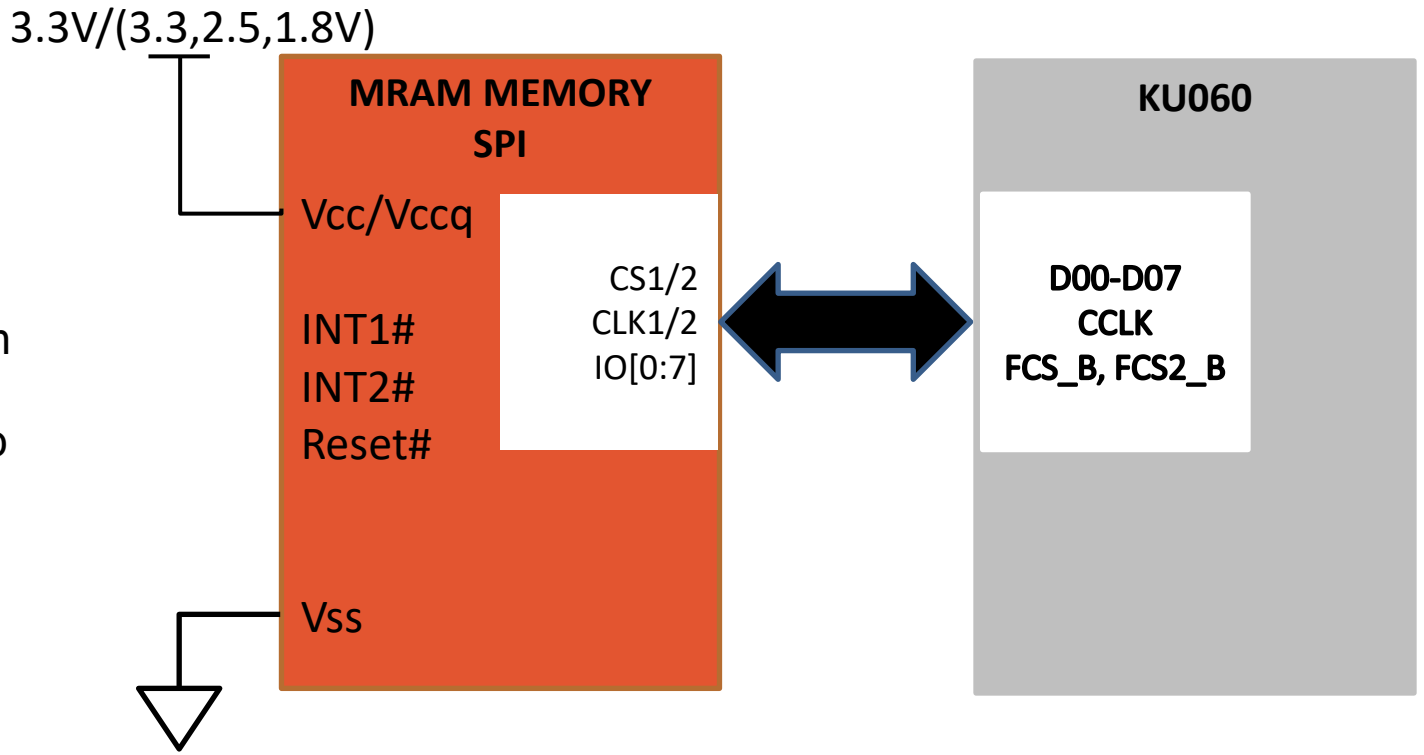
SPI Interface

Interface:

- UT8MRQRHxG – Dual Quad SPI bus operated

Operation:

- UT8MRQRHxG stores Versal configuration image
- Utilizes Master SPI configuration mode to auto load the image to the FPGA

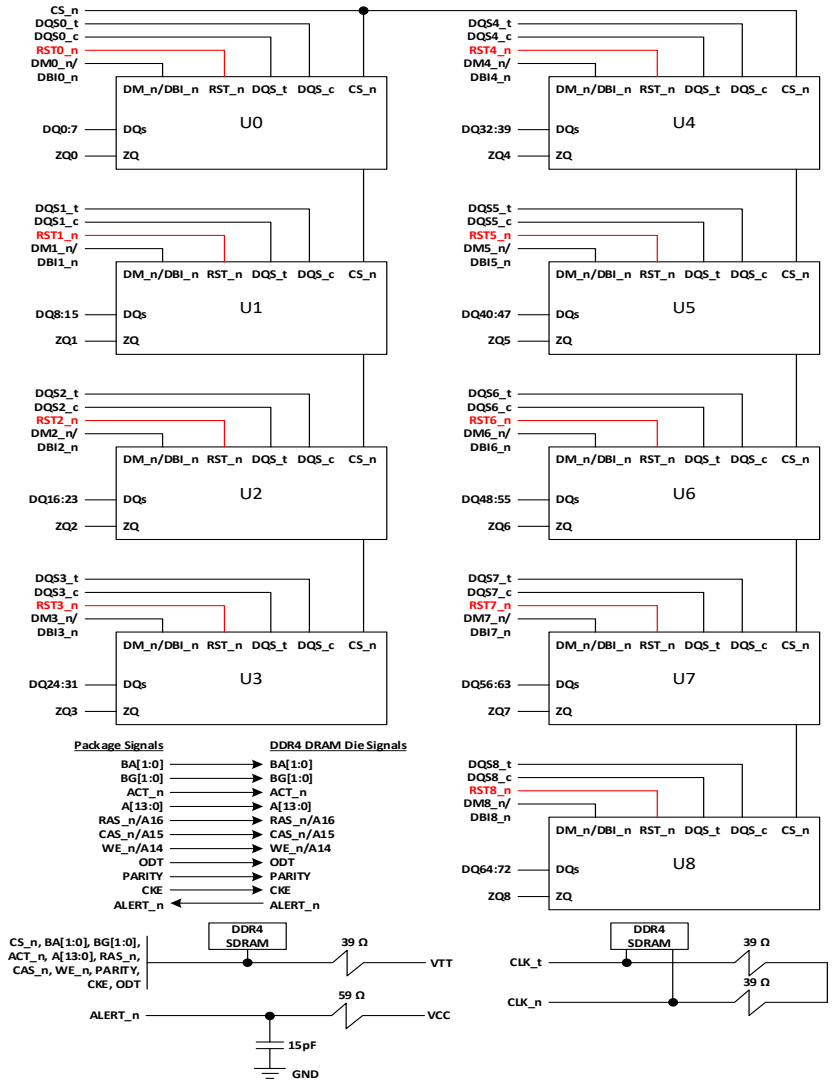


UT8SD4MQ2G72 DDR4 Memory

UT8SD4MQ2G72 - 18GB (16GB + 2GB ECC) DDR4

Product Details

Functional Block Diagram



Part Number	UT8SD4MQ2G72
Density	18GB (16GB + 2GB ECC)
Configuration	2G x 72 (9 die)
Read/Write time	220mW burst read/write power per die
Supply Voltage	1.2V V_{DD} & V_{DDQ}
Data Rate	2400 MT/s
Temp Range	-55^{0}C to +125^{0}C
Typical Power	ThetaJ-C = 4 °C/W
Package	266-pin PBGA, 15mm x 20mm x 1.9mm. 1.17gm and 1mm pitch
Operational Environment	
TID target:	100 krad
SEL Event Rate:	6.0E-8 events/device-day at GEO (LET from 37 to 82) @105C
SEU:	8.93E-12 Errors/Bit-Day
Qualification	Frontgrade Space PEM L2

UT8SD4MQ2G72 DDR4 Memory

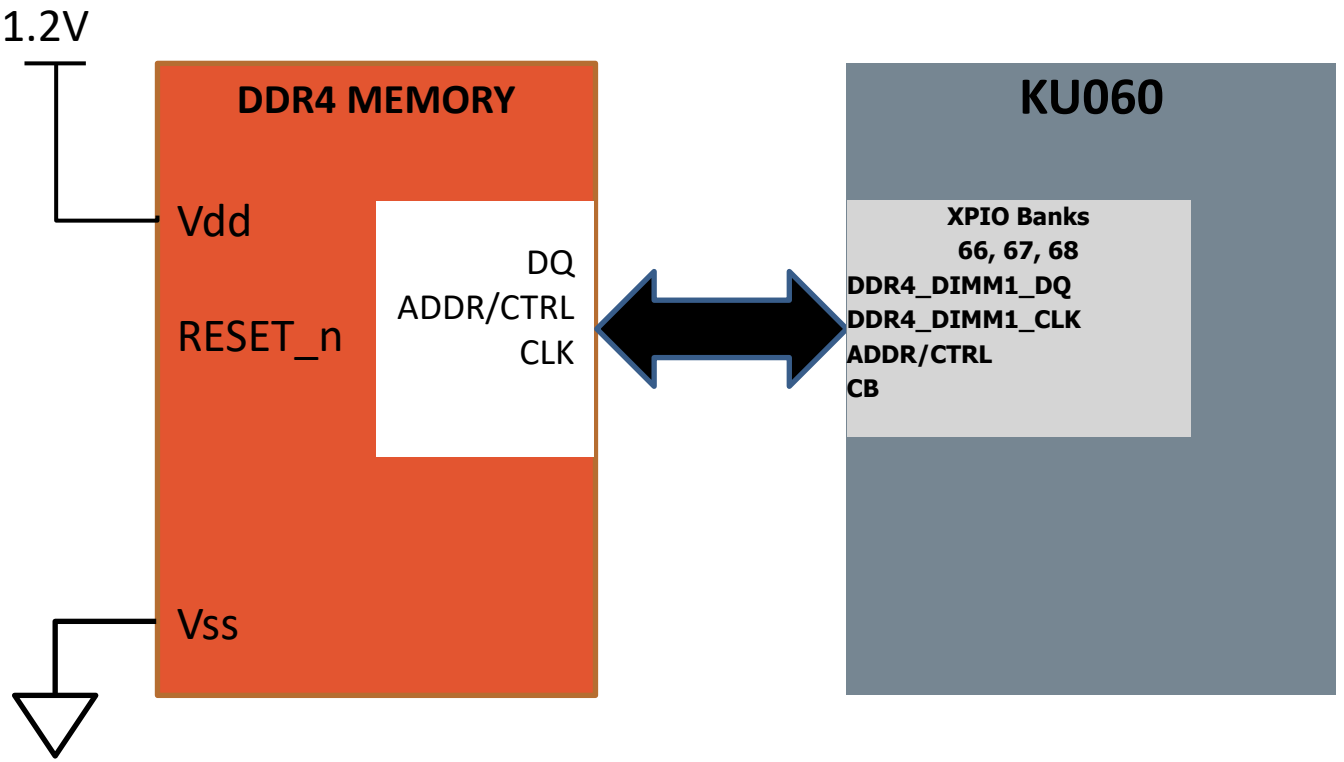
Interface

Interface:

- UT8SD4MQ2G72 – Standard DDR4 interface

Operation:

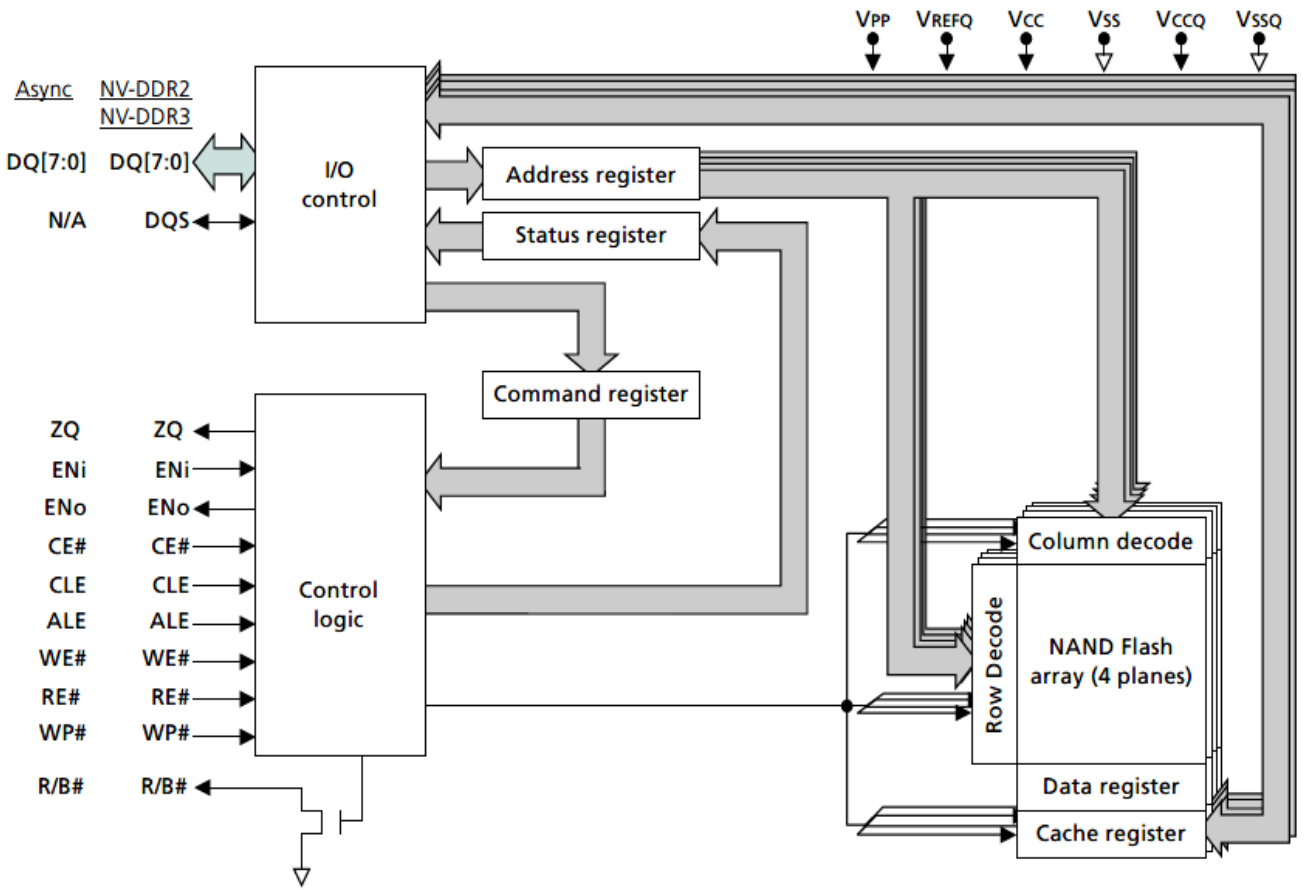
- UT8SD4MQ2G72 works with Versal integrated DDR4 Controller



UT81NDQ512G8T 4Tb NAND Flash

UT81NDQ512G8T 4Tb NAND Flash

Product Details



Part Number	UT81NDQ512G8T
SMD#	n/a
Density	4Tb
Configuration	4 Target, 8 LUN 64Gb x8 module
Page Size	18,592 bytes (TLC Mode)
Block Size	2304 Pages
Interface	ONFI 4.0 Compliant (132 ball footprint) Backward compatible to ONFI 2.x
Supply Voltage	+3.3V (core) and +1.2V or 1.8V (I/O)
Transaction Rate	Asyn Mode 5: 50MT/s/pin DDR2 Mode 8: 533 MT/s/pin DDR3 Mode 9: 667 MT/s/pin
Endurance	40K Program/Erase Cycles (SLC Mode) 3K Program/Erase Cycles (TLC Mode)
Data Retention	JESD47G compliant
Temp Range	-40°C to +85°C
Typical Power	150mW (per active die)
Package	JEDEC 132-PBGA, 12mm x 18mm x 1.4mm, 0.5g
Operational Environment	
TID:	30 - 50krad (Si) – Wafer lot RHA Qual Dependent
SEL:	<60 MeV-cm^2/mg @85°C
Qualifications	PEM-INST-001 (NASA EEE-INST-002) – Level 2

UT81NDQ512G8T, 4Tb NAND Flash

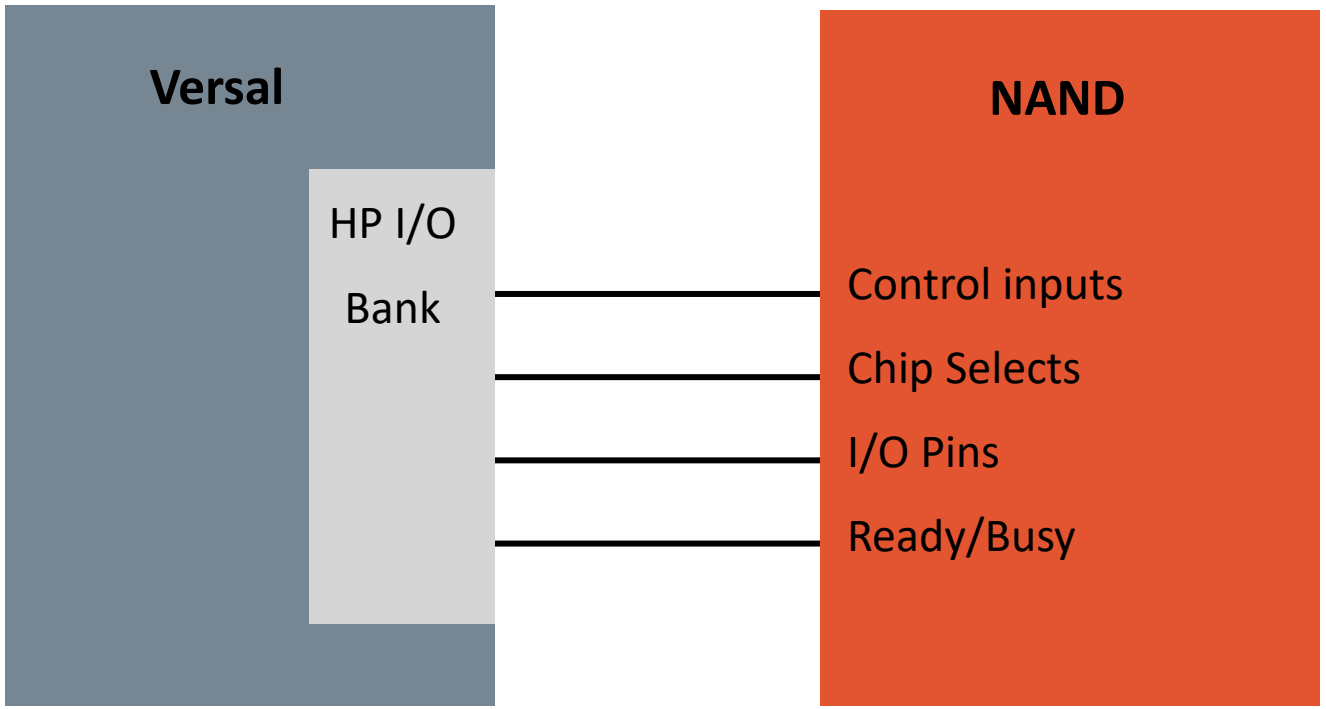
Interface

Interface:

- Recommend using HP I/O Banks to connect the NAND to the KUO60
- 8-bit operation can fit in one I/O bank
- 16-bit operation can fit in one I/O bank minus signals Eno, Eni, and Vpp

Operation:

- Will require NAND controller IP to interface to the NAND
- Recommend ONFi 4.0 or higher controller

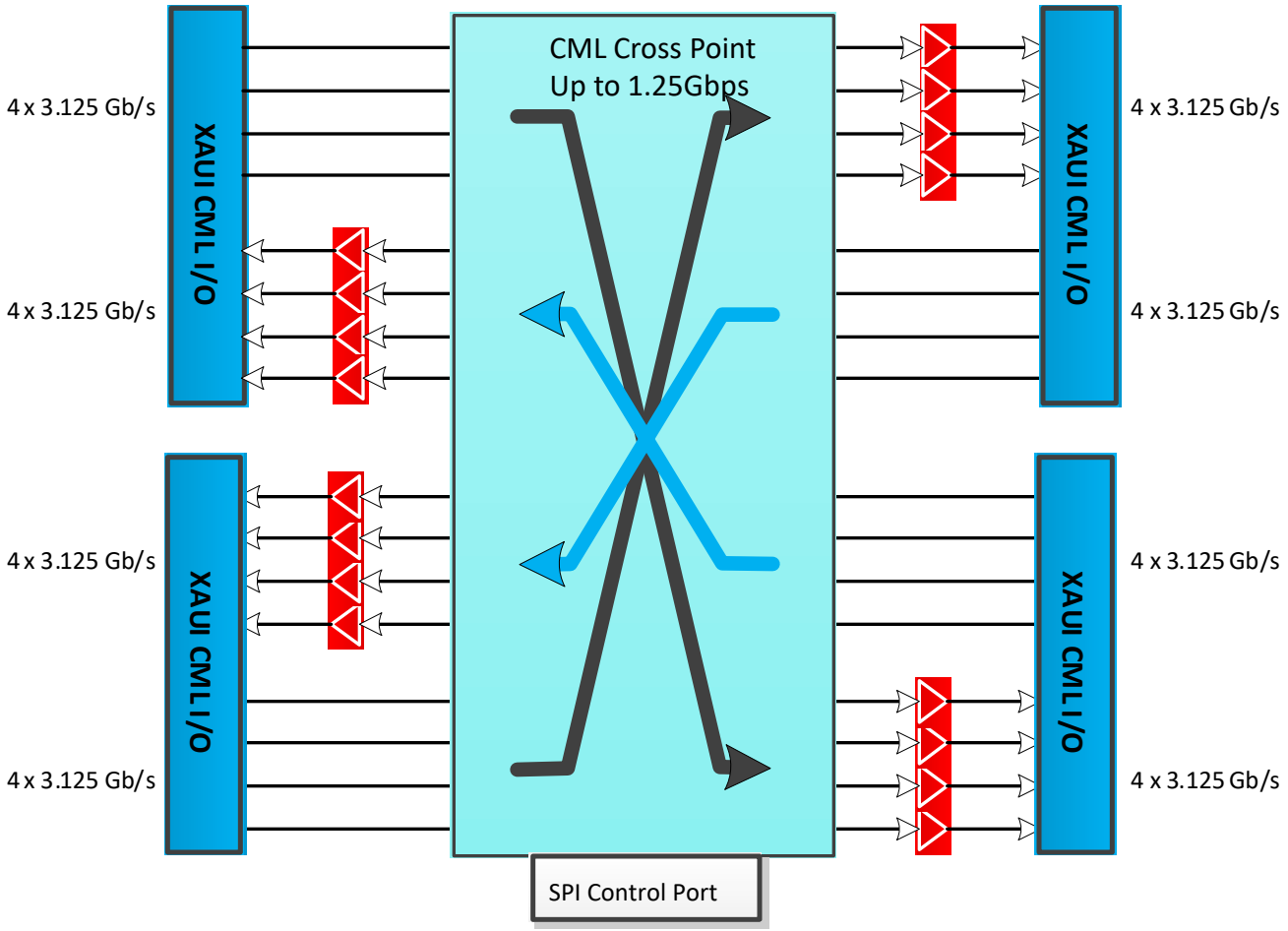


UT65CML8X8FD Crosspoint Switch

UT65CML8X8FD

8x8 High-Speed Crosspoint Switch Product Features

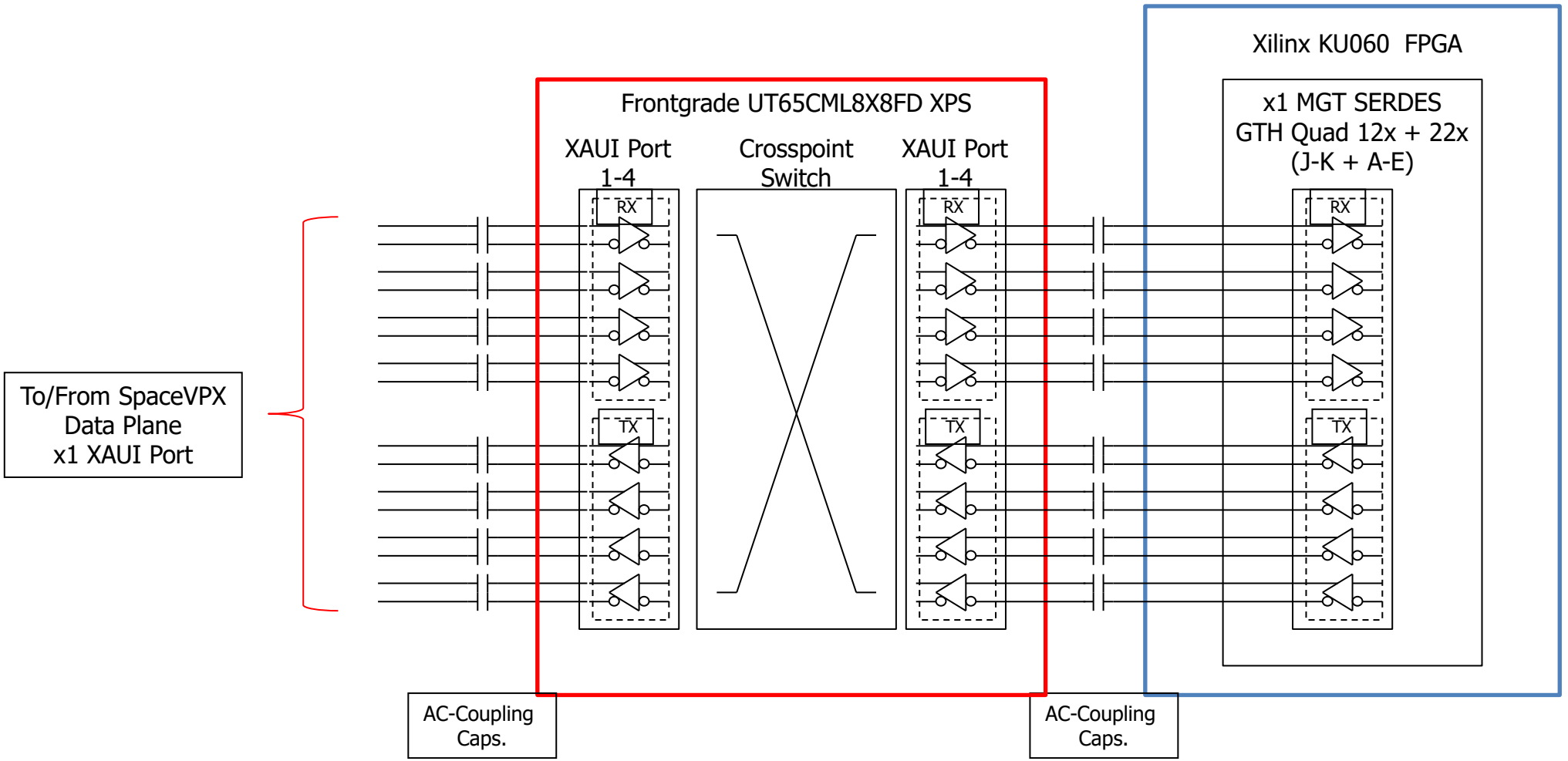
Functional Block Diagram



Part Number	UT65CML8X8FC
SMD#	5962-17213
Channels	8x8
Data Rate	3.125Gbps per channel (50Gbps total)
Supply Voltages	+1.2V Core[1], +1.2V-+1.8V CML, +2.5V SPI Port
Features	• 8 x 8, full duplex crosspoint switch matrix • Protocol independent • Low latency • Low channel-to-channel skew • SPI port control interface • Power down of unused lanes • Trimmable high-speed terminations
Process Technology	130nm CMOS
Typical Power	1.6W
Package	143 pin CLGA, CBGA, CCGA options 14.5 mm x 14.5 mm, 1mm pitch
Operational Environment	
Temp Range:	-55°C to +105°C
TID:	100 krad (Si)
SEL Immune:	LET ≤ 100 MeV-cm^2/mg @105°C
Qualifications	QML-Q, V (pending)

Versal™ FPGA + UT65CML8X8FD XPS

SpaceVPX Data Plane Interface Application



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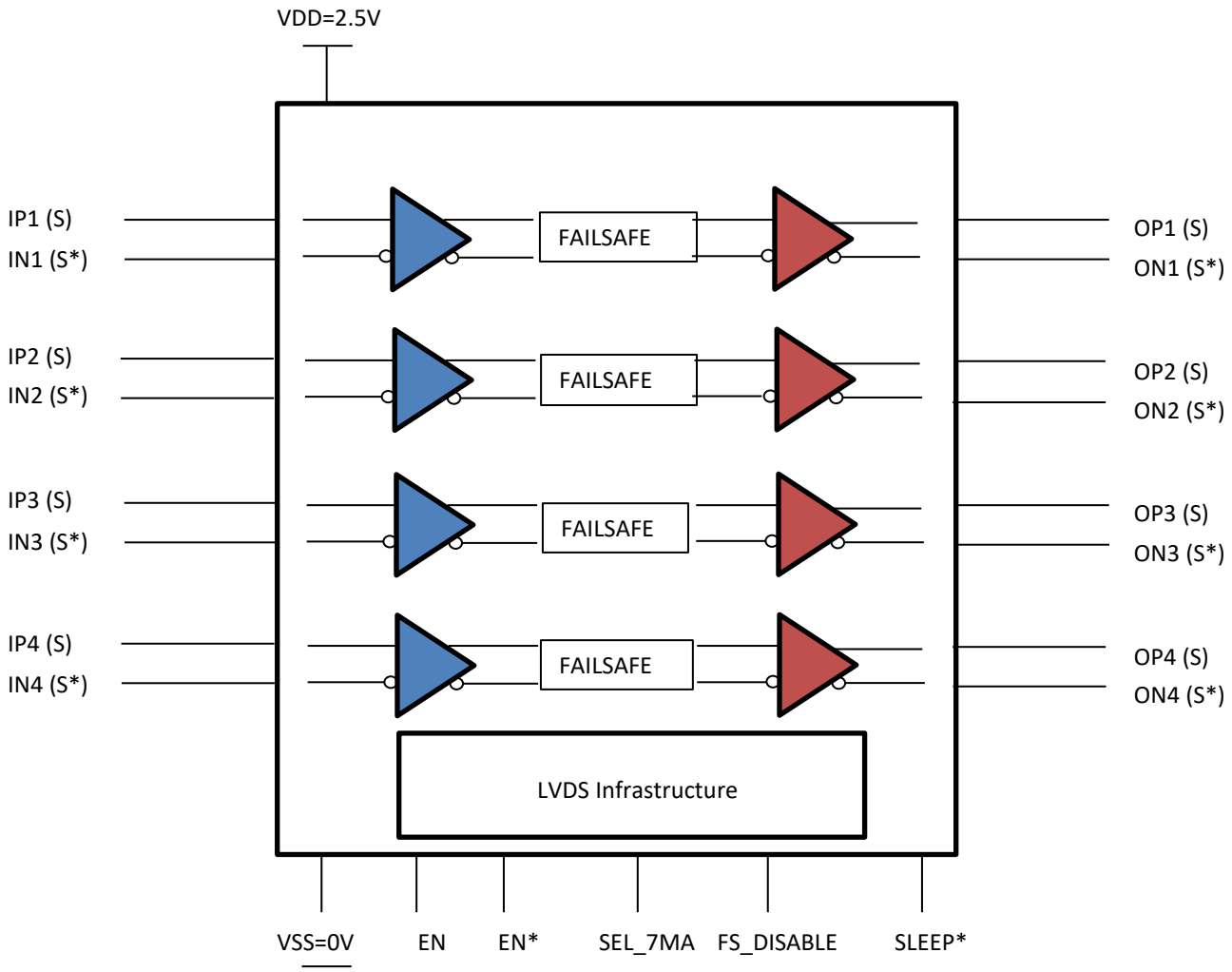
UT54LVDS454 1.25 Gbps Quad LVDS Repeater

UT54LVDS454 Quad Repeater

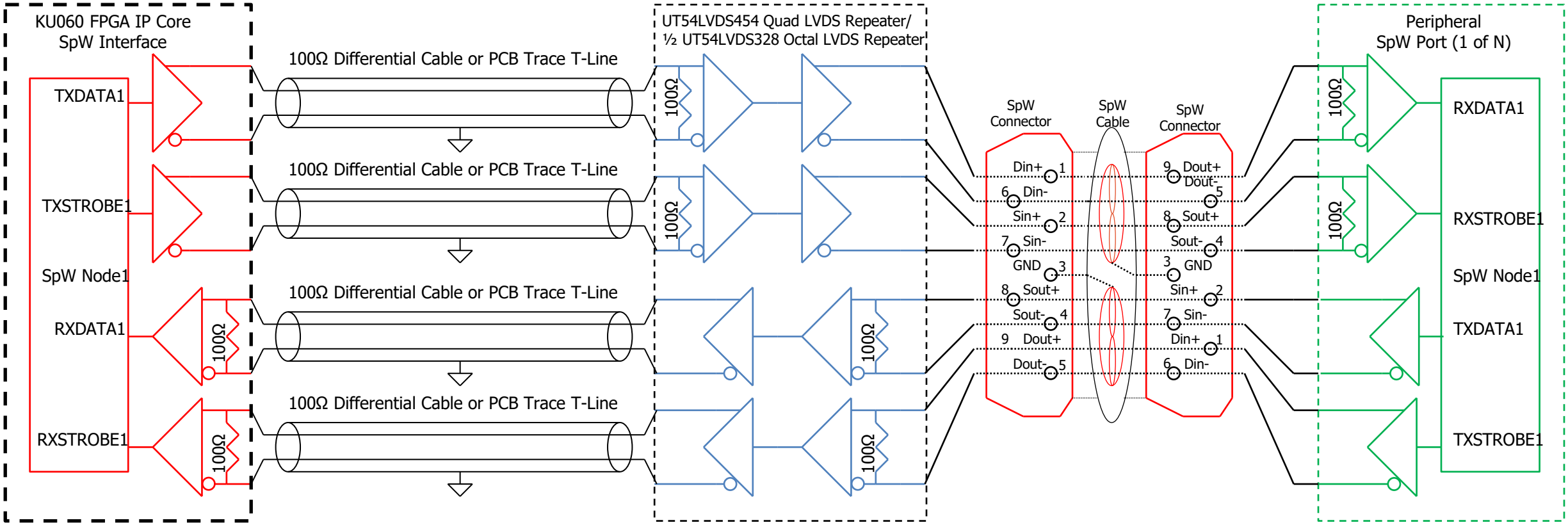
High-Speed (1.25Gbps) LVDS Quad Repeater Product Details

Functional Block Diagram



Part Number	UT54LVDS454
SMD#	5962-21211
Channels	Quad Repeater
Data Rate	1.25Gbps per channel
Supply Voltage	2.5V single supply
Features	• Selectable drive strength • Cold sparing all pins • Enable/Disable input to disable LVDS drivers • Sleep mode for ultra-low power dissipation • Fail-safe function for loss-of-signal detection
Process Technology	130nm (LP)
Typical Power	170mW
Package	72 pin CLGA 9mm x 10mm, 1mm pitch
Operational Environment	
Temp Range:	-55°C to +105°C
TID:	100 krad (Si)
SEL Immune:	LET ≤ 100 MeV-cm^2/mg @105°C
Qualifications	QML-Q, -V (pending)

SpW/LVDS Repeater: x1 SpW Port



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LVDS Repeaters For SpW Interfacing & KU060 FPGA I/O Protection

Frontgrade UT54LVDS328 400 Mbps Octal LVDS Repeater Device Features

- Data rates up to 400.0 Mbps per channel / 200 MHz clock channel
- 3.3V power supply / 3.5mA LVDS TX output drive current / Total integrated dose (TID): 1Mrad(Si)
- Extends SpW channel reach - x1 UT54LVDS328 octal LVDS repeater supports x2 SpW ports
- Protects KU060 FPGA LVDS I/Os: General High-Speed Serial LVDS, ADC JESD204, and SpW Interfaces
- Cold sparing all pins / 48-lead CFP package

Frontgrade UT54LVDS454 1.25 Gbps Dual, Full-Duplex / Quad, Simplex LVDS Repeater Device Features

- Data rates up to 1.25 Gbps per channel / protocol independent
- 2.5V power supply / Selectable 3.5mA or 7.0mA TX output drive currents / Total integrated dose (TID): 100krad(Si)
- Extends SpW channel reach - x1 UT54LVDS454 quad LVDS repeater supports x1 SpW port
- Protects KU060 FPGA LVDS I/Os: General High-Speed Serial LVDS, ADC JESD204, and SpW Interfaces
- Cold sparing all pins / 71-land C-CGA/C-LGA package

KU060 FPGA to LVDS Repeater Design Considerations

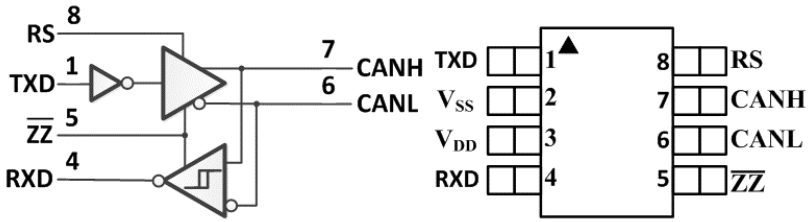
- SpW Interfacing: SpW IP Cores are Available for the KU060 FPGA
- https://www.xilinx.com/products/intellectual-property/1-12nthtb.html / https://soc-e.com/spacewire-ip-core/
- Frontgrade LVDS Repeaters Support SpW Interfacing to the KU060 FPGA Once the KU060 I/Os are Configured as a SpW Port or Ports
- Frontgrade LVDS Repeaters Also Protect KU060 FPGA LVDS I/Os: General High-Speed Serial LVDS, ADC JESD204, and SpW Interfaces

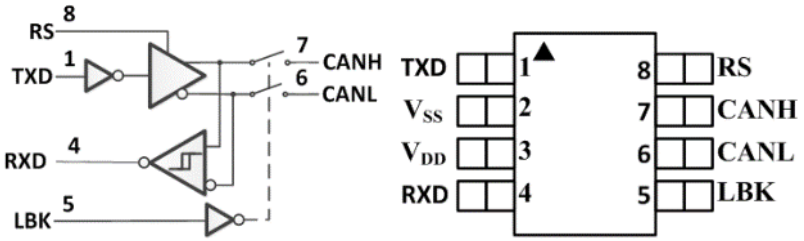
UT64CAN3330, 3331 and 3332
CAN Transceivers

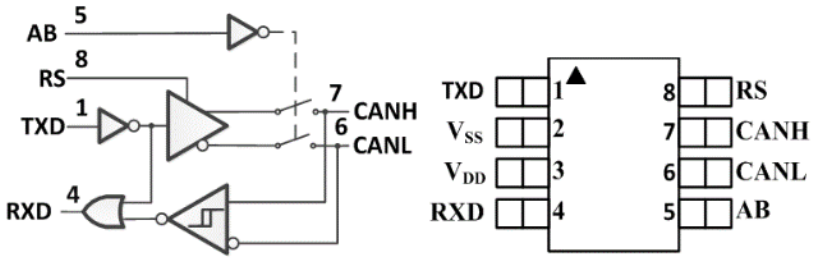
CAN Transceivers (XCVRs)

Product Details

Functional Block Diagrams

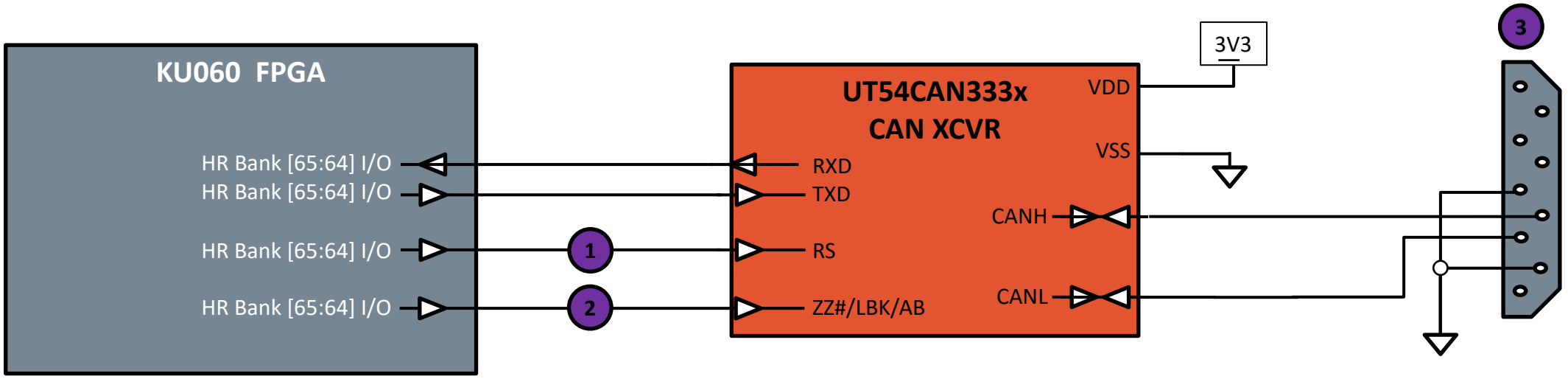






Part Number	UT64CAN3330	UT64CAN3331	UT64CAN3332
SMD#	5962-15232	5962-15232	5962-15232
Supply Voltage	+3.3V	+3.3V	+3.3V
Digital I/O	+3V (5V Tolerant)		
Baud Rate	10Kbps to 8Mbps		
Differential input impedance	40KΩ - 100KΩ		
Differential input capacitance	25pF (max)		
Worst case loop propagation delay	85ns (max) to 1650ns (max) depending on selected CAN signal slew-rate		
CAN Bus output drive	-50mA to 50mA		
Package	8-lead FP		
Operational Environment			
Temp Range:	-55°C to +125°C		
TID:	100 krad (Si)		
SEL Immune:	LET <=141 MeV-cm^2/mg		
Qualifications	QML-Q, V		

KU060 CAN Transceiver Interface



KU060 CAN Transceiver Interface

Notes

1. The RS pin on the UT64CAN333x series CAN transceivers provides three functional modes of operation:
   - High-speed: The high-speed mode of operation is selected by connecting RS (pin 8) directly to ground, allowing the driver output to achieve a baud rate up to 8 Mbps
   - Slope control: The rise and fall slopes are adjusted by connecting a resistor to ground at RS (pin 8). The slope of the driver output signal is proportional to the pin's output current. This slope control is implemented with an external resistor value between 10 kΩ to 100 kΩ, where these resistor values control the slew rates between ~2.0 V/µs to ~20 V/µs, respectively
   - Low-power standby mode: If RS is set to a high-level input (> 0.75*VDD), the transceiver enters a low current, listen only mode of operation. In this mode, the CAN bus driver is disabled and the receiver remains active. The CAN controller has ability to disable low-power standby mode once bus activity resumes
2. Along with the common functionality described, the UT64CAN333x family of transceivers includes three members, each with a unique mode of operation.
   - The UT64CAN3330, Figure 1, provides the option to place the transceiver into a low power sleep mode to conserve power when CAN activity is suspended. Sleep mode disables the driver and receiver circuit when the ZZ pin is biased ≤ VIL. The part resumes operations when the ZZ pin is biased ≥ VIH.
   - The UT64CAN3331, Figure 2, provides the option to isolate the transceiver bus connections to permit local node diagnostics, without interrupting operations on the bus. Diagnostic Loopback mode is enabled when the LBK pin is biased ≥ VIH. Diagnostic Loopback mode is disabled when the LBK pin is biased ≤ VIL. In the Diagnostic Loopback mode, the CANH/CANL output is placed in the recessive mode. Also, the connection between TXD and RXD is made through the mode logic and connection and the connections for TXD and RXD are isolated from CANH/CANL.
   - The UT64CAN3332, Figure 3, provides the option to automatically synchronize the baud rate of the transceiver by matching the bit timing to the traffic on the bus. The Auto Baud Loopback mode is enabled when the AB pin is biased ≥ VIH. Auto Baud Loopback mode is disabled when the AB pin is biased ≤ VIL. In the Auto-Baud mode, the CANH/CANL output is placed in the recessive mode.
3. Program will dictate the off-board interface and connector requirements. DB9 based configuration is proposed.

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THANK YOU