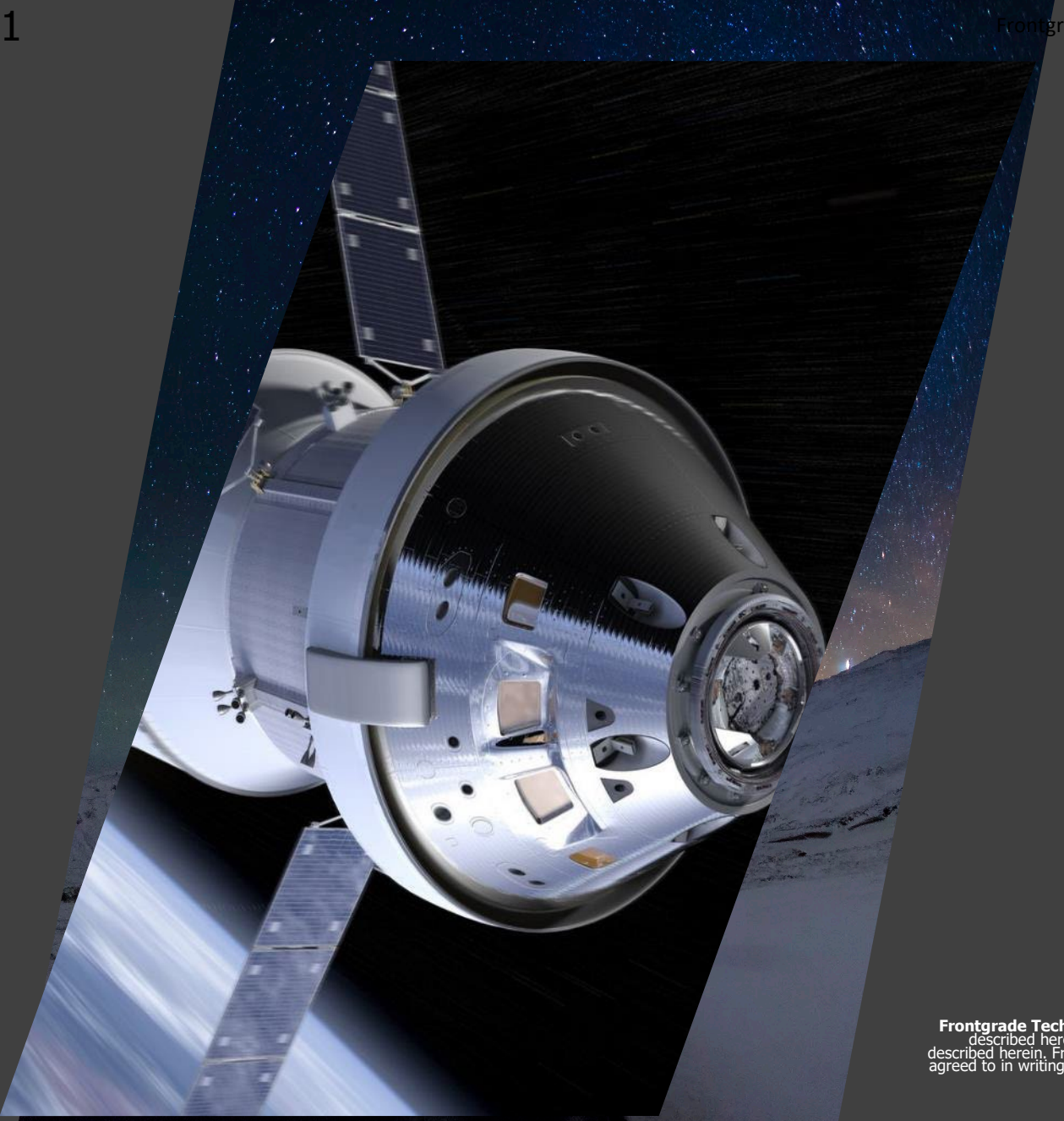
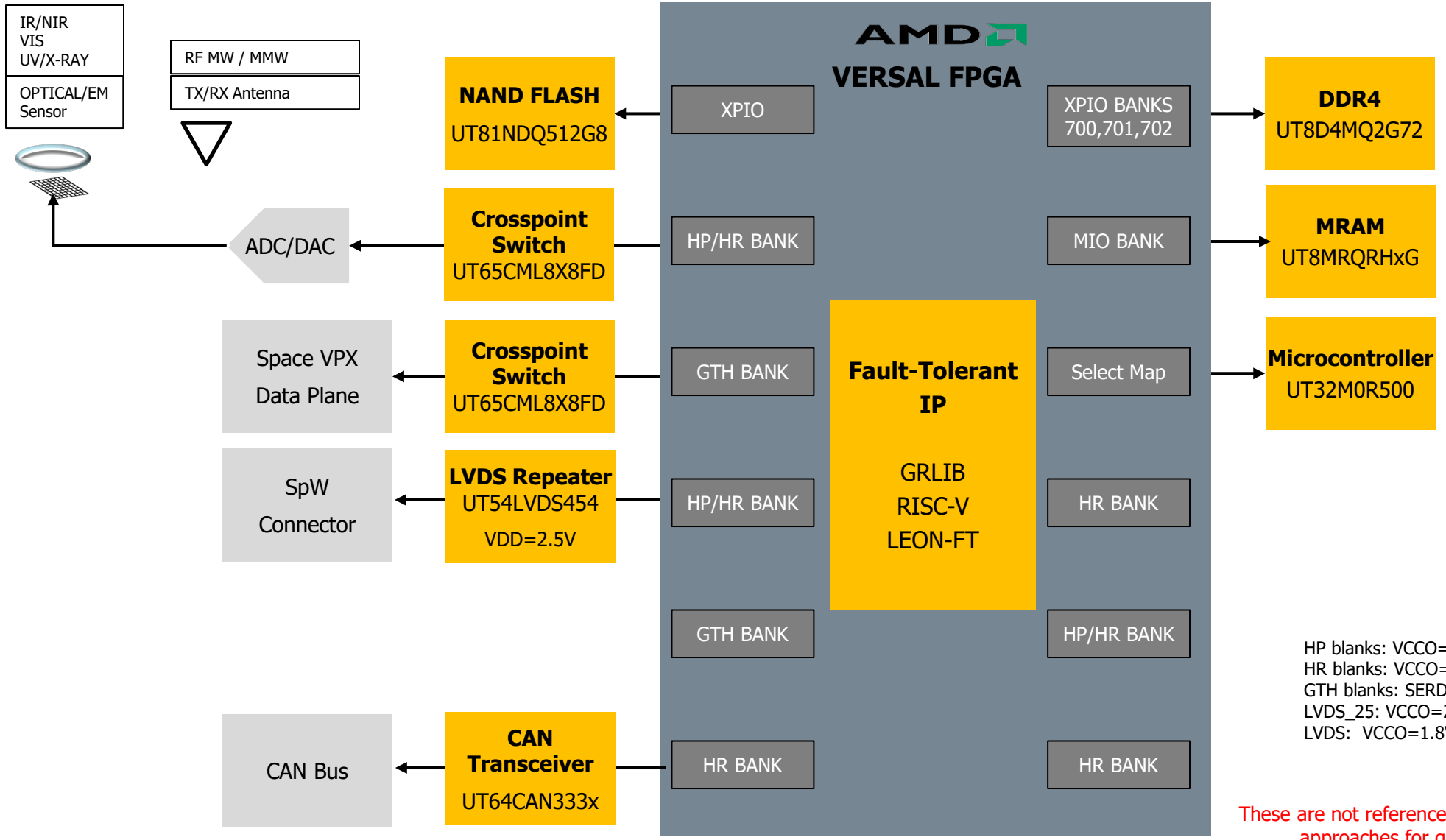


AMD Versal™ VSC1902 + Frontgrade Ecosystem Design Examples

January 2025

Frontgrade Versal FPGA Ecosystem



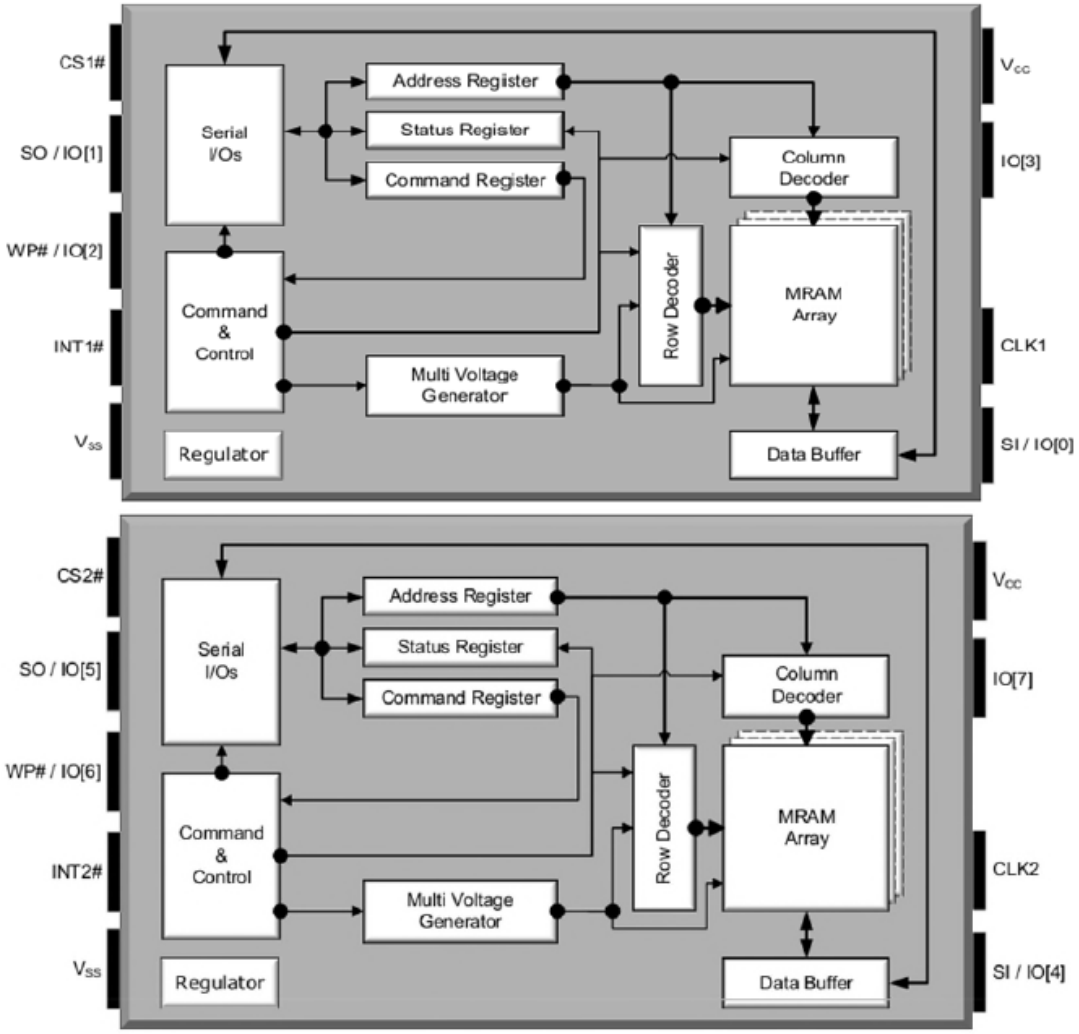
HP blanks: VCCO=1.0V-1.8V
HR blanks: VCCO=1.2V-3.3V
GTH blanks: SERDES (Gbps)
LVDS_25: VCCO=2.5V (HR)
LVDS: VCCO=1.8V (HP)

These are not reference designs. They are conceptual approaches for guidance purposes only.
For more information, please contact us at Frontgrade.com

UT8MRQxG MRAM Memory

MRAM Memory
Product Details

Functional Block Diagram
(Dual Quad SPI Interface)



Part Number	UT8MRQRHxG
Density	1,2,4,8 Gb
Interface	SPI
Configuration	2x Quad
Supply Voltage	+3.3V core; 1.8, 2.5V, 3.3V IO supplies
Write Endurance	10^{16} write cycles
Data Retention	> 10 years @ 85°C
Process Technology	22nm pMTJ STT
Temp Range	-40°C to +125°C
Package	224-ball FBGA (20x20 mm)
Operational Environment	
TID:	100 krad (Si)
SEL:	78 MeV-cm^2/mg @105°C, 2.7V
Qualifications	PEM L2, L1

UT8MRQxG MRAM Memory

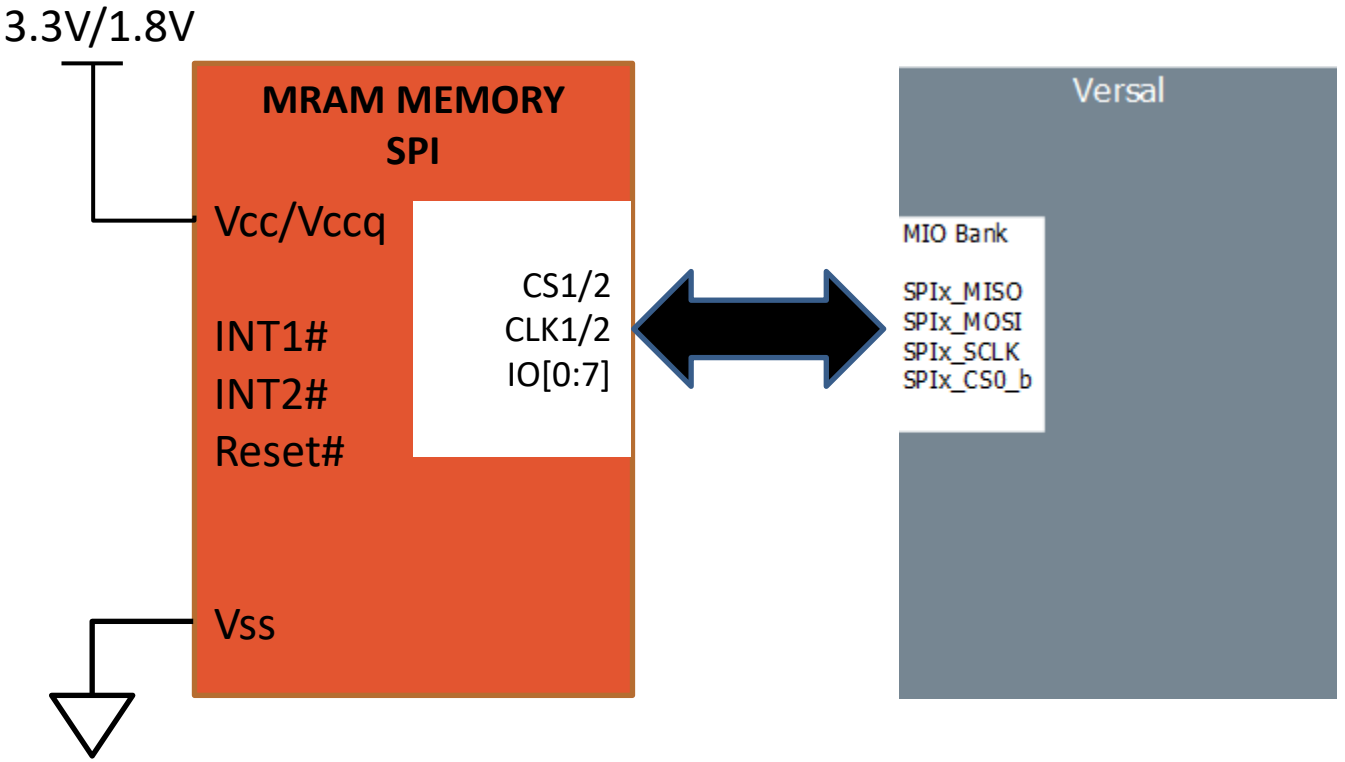
SPI Interface

Interface:

- UT8MRQRHxG – Dual Quad SPI bus operated

Operation:

- UT8MRQRHxG stores Versal configuration image
- Utilizes Master SPI configuration mode to auto load the image to the FPGA



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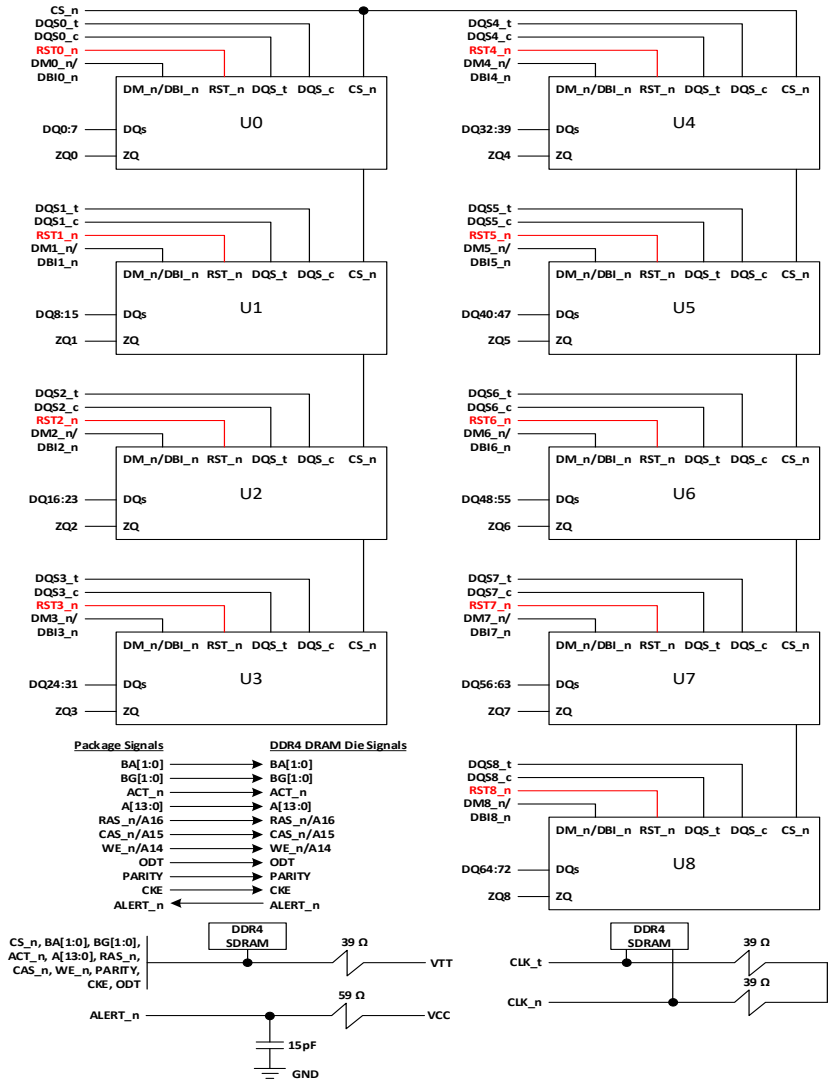
UT8SD4MQ2G72 DDR4 Memory

UT8SD4MQ2G72 - 18GB (16GB + 2GB ECC) DDR4

Product Details

Functional Block Diagram



Part Number	UT8SD4MQ2G72
Density	18GB (16GB + 2GB ECC)
Configuration	2G x 72 (9 die)
Read/Write time	220mW burst read/write power per die
Supply Voltage	1.2V V_{DD} & V_{DDQ}
Data Rate	2400 MT/s
Temp Range	-55^{0}C to +125^{0}C
Typical Power	ThetaJ-C = 4 °C/W
Package	266-pin PBGA, 15mm x 20mm x 1.9mm. 1.17gm and 1mm pitch
Operational Environment	
TID target:	100 krad
SEL Event Rate:	6.0E-8 events/device-day at GEO (LET from 37 to 82) @105C
SEU:	2.23E-14 Errors/Bit-Day
Qualification	Frontgrade Space PEM L2

UT8SD4MQ2G72 DDR4 Memory

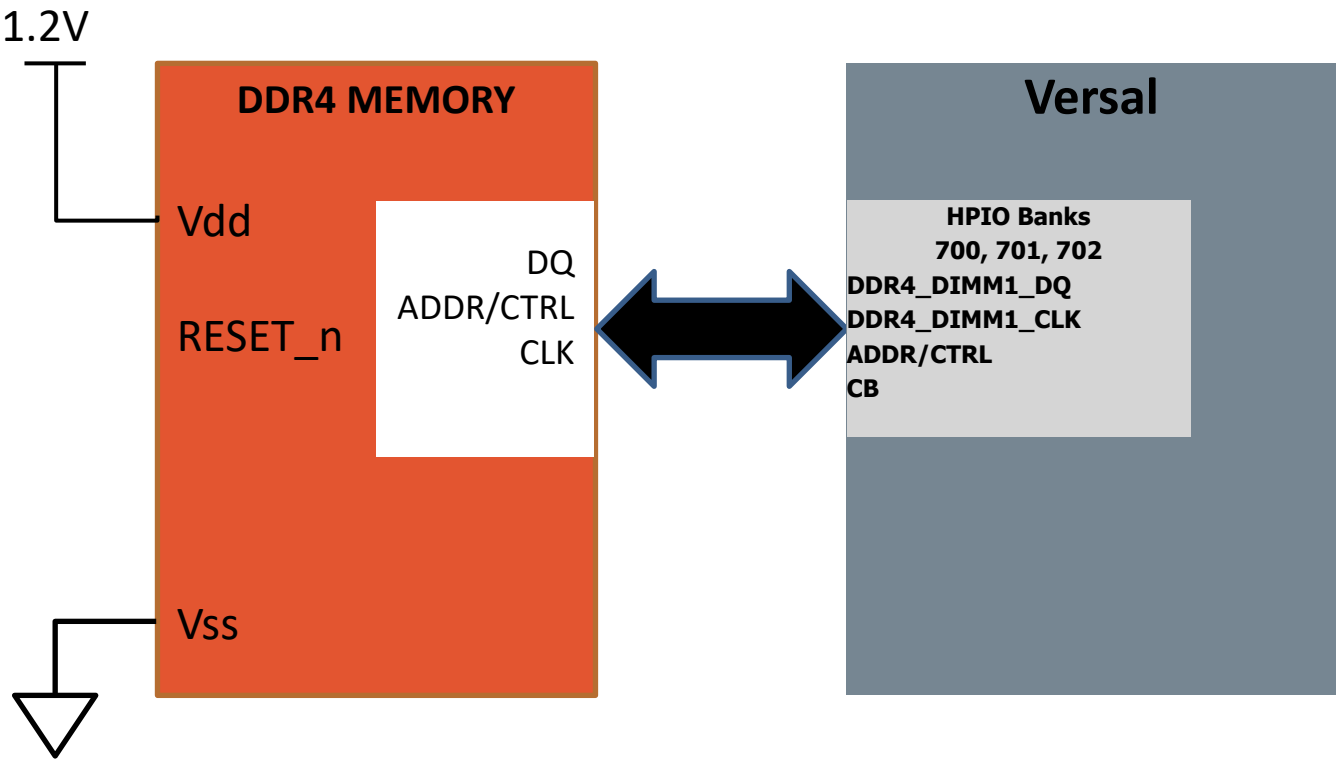
Interface

Interface:

- UT8SD4MQ2G72 – Standard DDR4 interface

Operation:

- UT8SD4MQ2G72 works with Versal integrated DDR4 Controller



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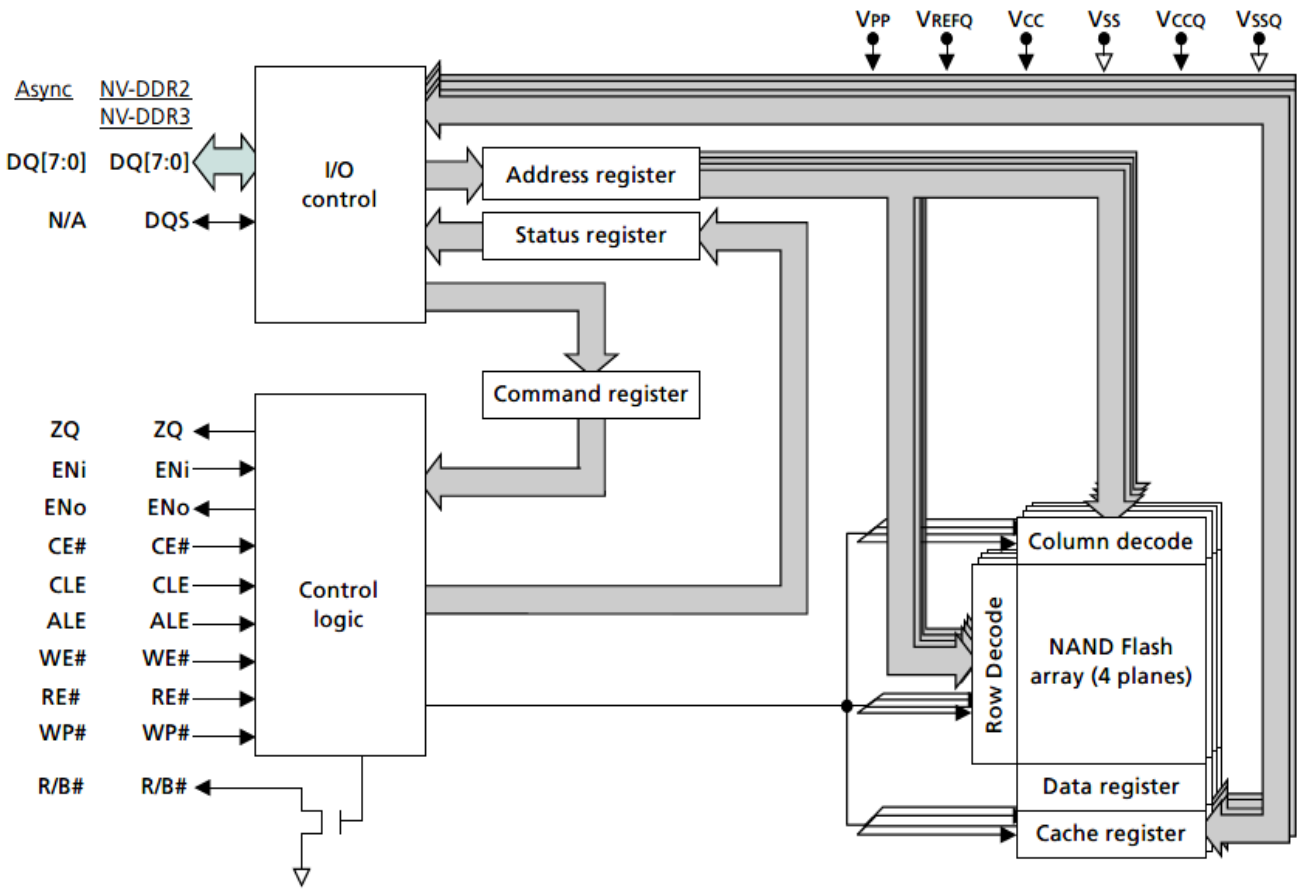
UT81NDQ512G8T 4Tb NAND Flash

FRONTGRADE

UT81NDQ512G8T 4Tb NAND Flash

Product Details



Part Number	UT81NDQ512G8T
SMD#	n/a
Density	4Tb
Configuration	4 Target, 8 LUN 64Gb x8 module
Page Size	18,592 bytes (TLC Mode)
Block Size	2304 Pages
Interface	ONFI 4.0 Compliant (132 ball footprint) Backward compatible to ONFI 2.x
Supply Voltage	+3.3V (core) and +1.2V or 1.8V (I/O)
Transaction Rate	Asyn Mode 5: 50MT/s/pin DDR2 Mode 8: 533 MT/s/pin DDR3 Mode 9: 667 MT/s/pin
Endurance	40K Program/Erase Cycles (SLC Mode) 3K Program/Erase Cycles (TLC Mode)
Data Retention	JESD47G compliant
Temp Range	-40°C to +85°C
Typical Power	150mW (per active die)
Package	JEDEC 132-PBGA, 12mm x 18mm x 1.4mm, 0.5g
Operational Environment	
TID:	30 - 50krad (Si) – Wafer lot RHA Qual Dependent
SEL:	<60 MeV-cm^2/mg @85°C
Qualifications	PEM-INST-001 (NASA EEE-INST-002) – Level 2

UT81NDQ512G8T, 4Tb NAND Flash

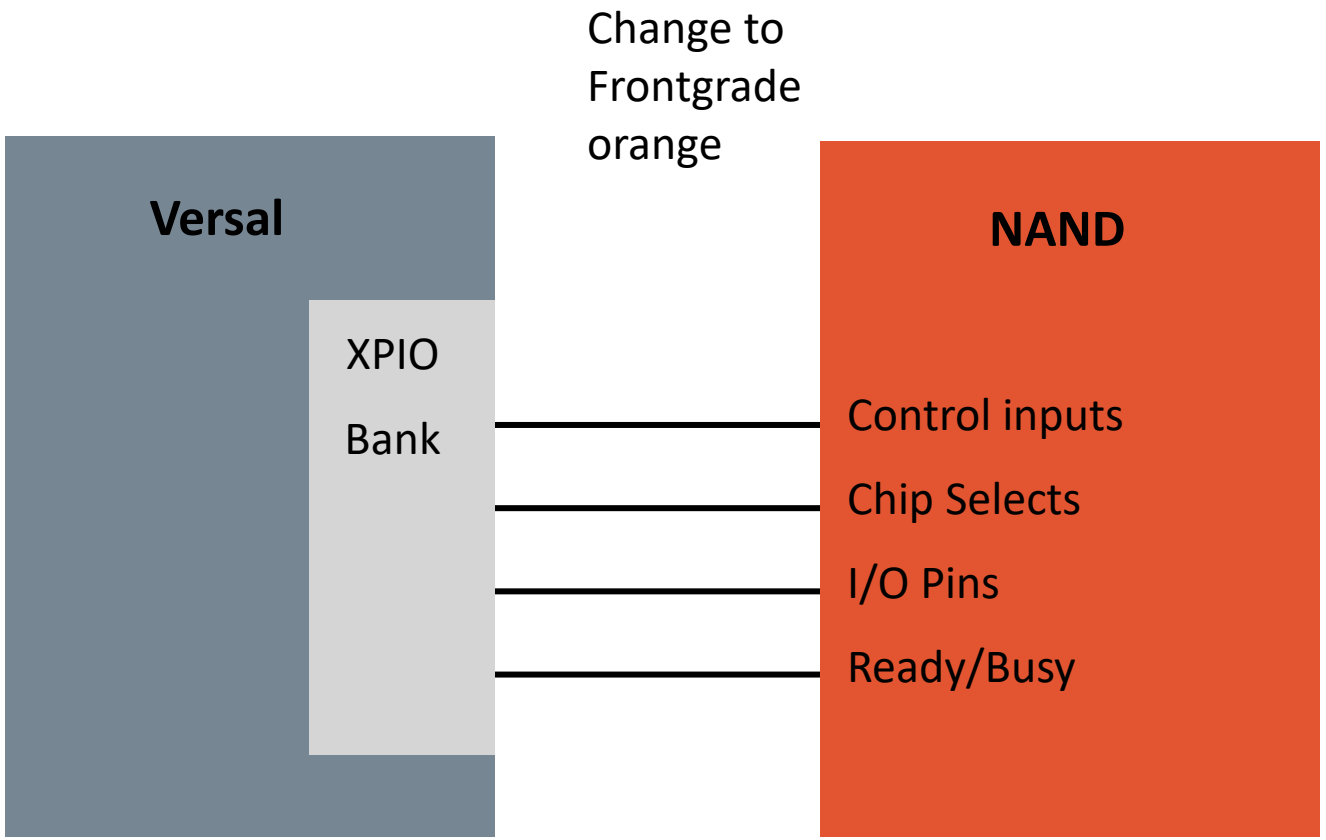
Interface

Interface:

- Recommend using XP I/O Banks to connect the NAND to the Versal
- 8-bit operation can fit in one I/O bank
- 16-bit operation can fit in one I/O bank minus signals Eno, Eni, and Vpp

Operation:

- Will require NAND controller IP to interface to the NAND
- Recommend ONFi 4.0 or higher controller



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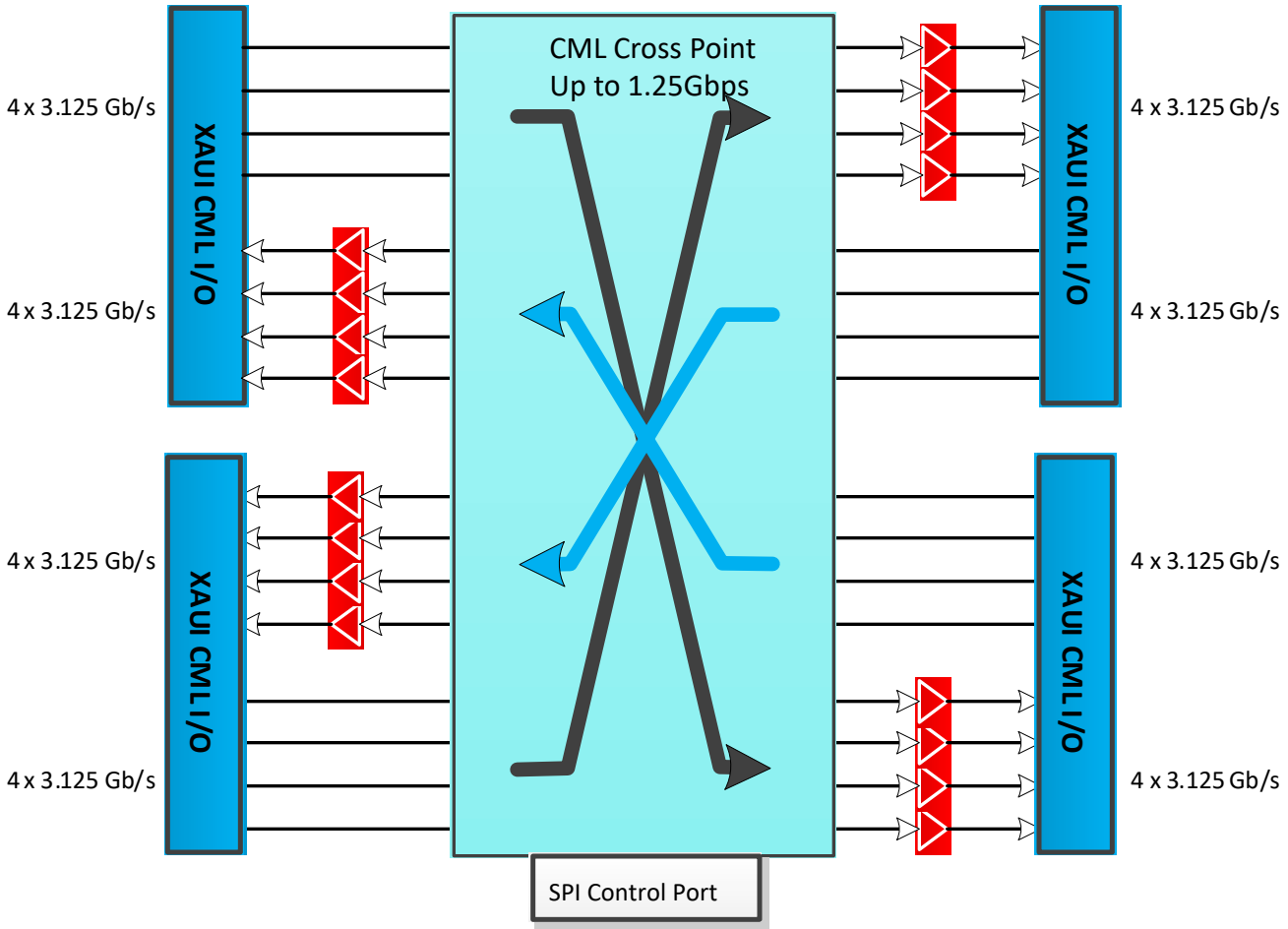
UT65CML8X8FD 3.125 Gbps Crosspoint Switch (XPS)

UT65CML8X8FD

8x8 High-Speed Crosspoint Switch Product Features

Functional Block Diagram



Part Number	UT65CML8X8FC
SMD#	5962-17213
Channels	8x8
Data Rate	3.125Gbps per channel (50Gbps total)
Supply Voltages	+1.2V Core[1], +1.2V-+1.8V CML, +2.5V SPI Port
Features	• 8 x 8, full duplex crosspoint switch matrix • Protocol independent • Low latency • Low channel-to-channel skew • SPI port control interface • Power down of unused lanes • Trimmable high-speed terminations
Process Technology	130nm CMOS
Typical Power	1.6W
Package	143 pin CLGA, CBGA, CCGA options 14.5 mm x 14.5 mm, 1mm pitch
Operational Environment	
Temp Range:	-55°C to +105°C
TID:	100 krad (Si)
SEL Immune:	LET ≤ 100 MeV-cm^2/mg @105°C
Qualifications	QML-Q, V (pending)

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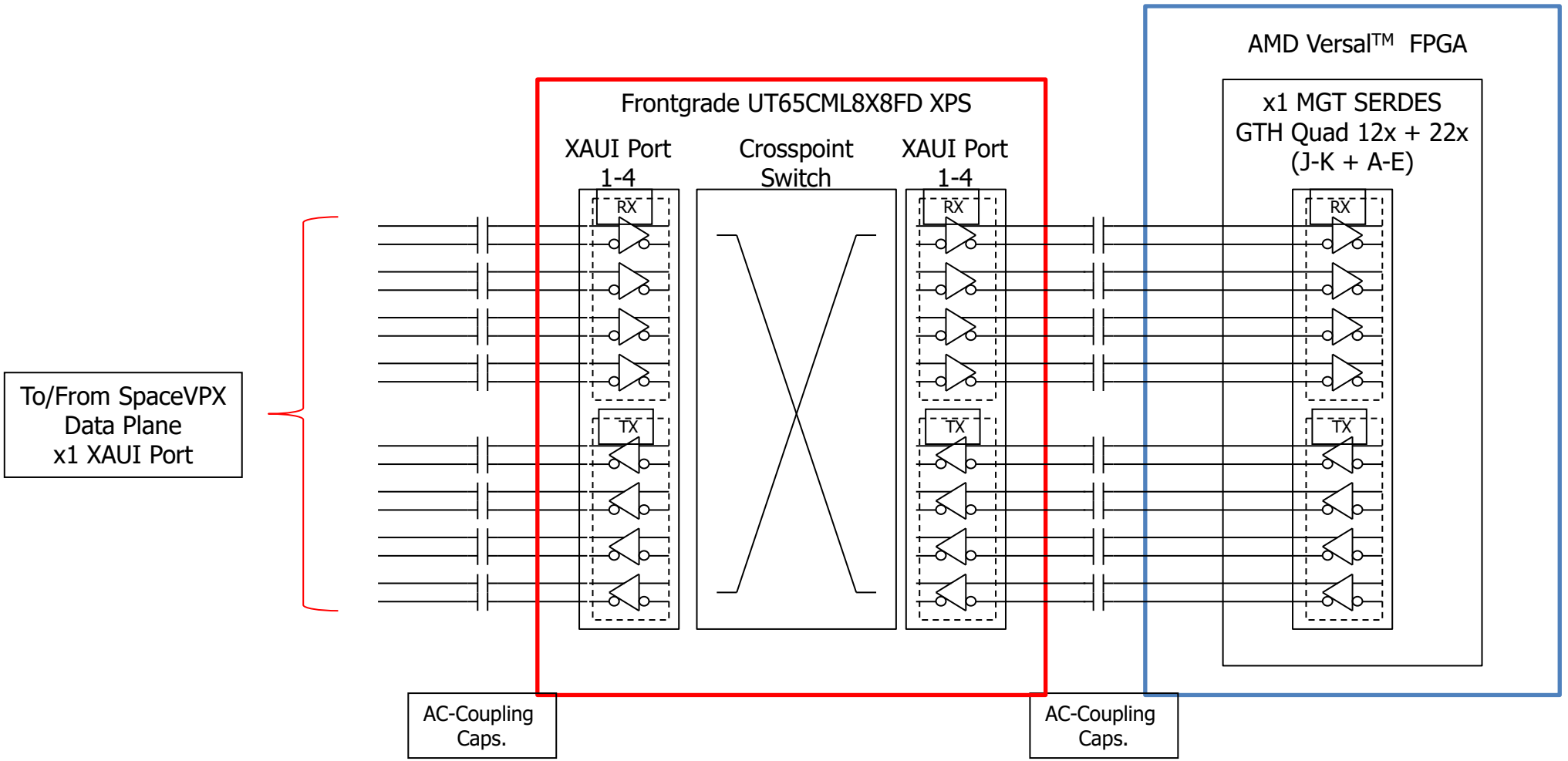
Versal™ FPGA + UT65CML8X8FD XPS

SpaceVPX Data Plane Interface Application



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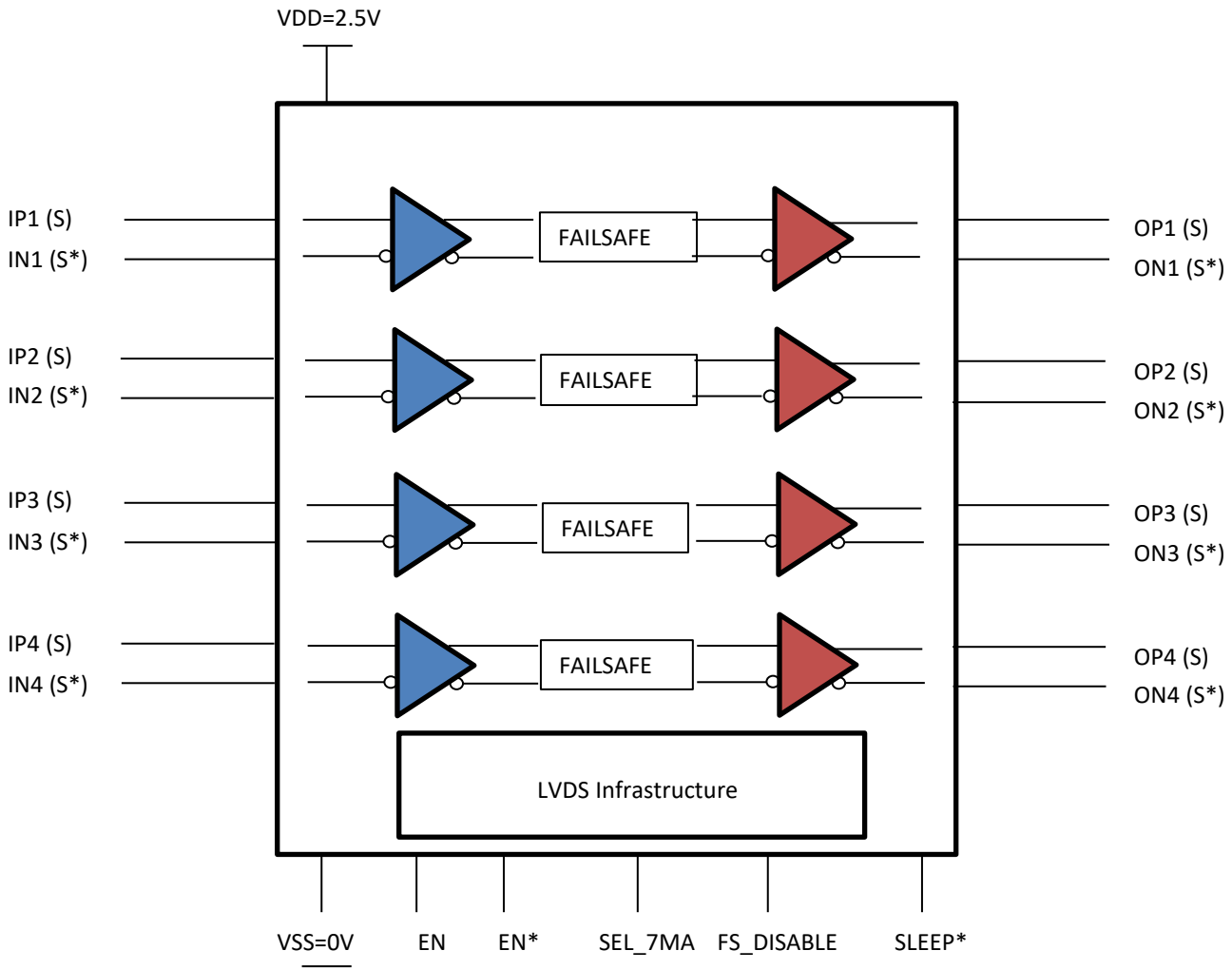
UT54LVDS454 1.25 Gbps Quad LVDS Repeater

UT54LVDS454 Quad Repeater

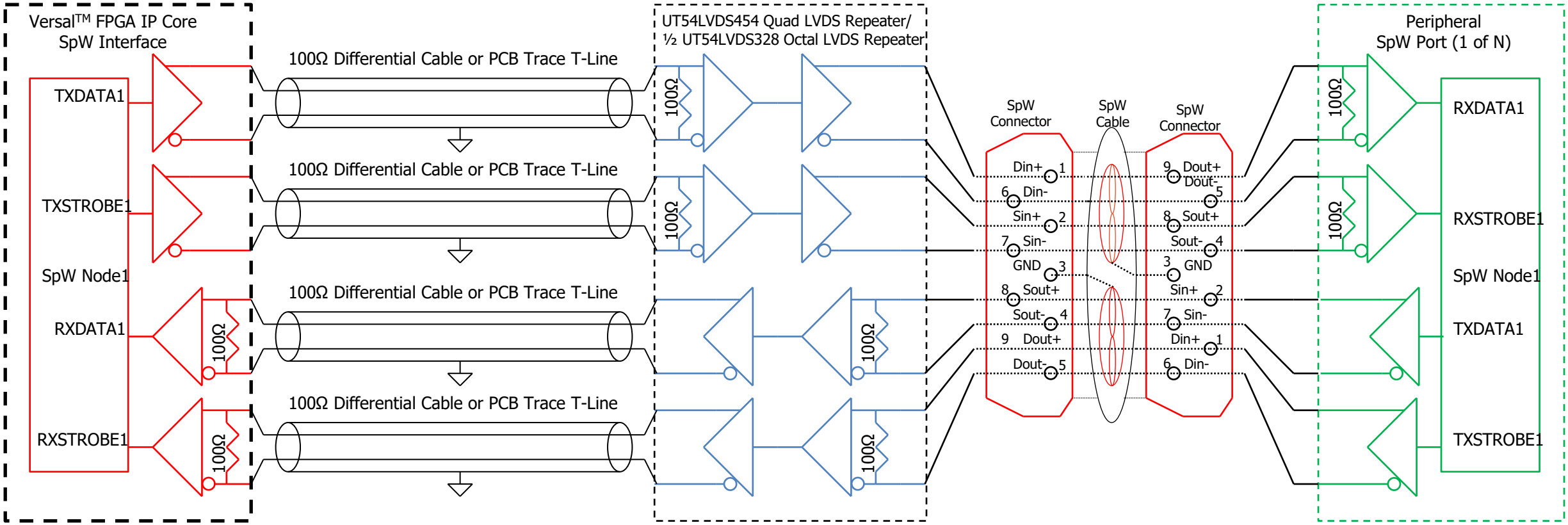
High-Speed (1.25Gbps) LVDS Quad Repeater Product Details

Functional Block Diagram



Part Number	UT54LVDS454
SMD#	5962-21211
Channels	Quad Repeater
Data Rate	1.25Gbps per channel
Supply Voltage	2.5V single supply
Features	• Selectable drive strength • Cold sparing all pins • Enable/Disable input to disable LVDS drivers • Sleep mode for ultra-low power dissipation • Fail-safe function for loss-of-signal detection
Process Technology	130nm (LP)
Typical Power	170mW
Package	72 pin CLGA 9mm x 10mm, 1mm pitch
Operational Environment	
Temp Range:	-55°C to +105°C
TID:	100 krad (Si)
SEL Immune:	LET ≤ 100 MeV-cm^2/mg @105°C
Qualifications	QML-Q, -V (pending)

SpW/LVDS Repeater: x1 SpW Port



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LVDS Repeaters For SpW Interfacing & AMD Versal™ FPGA I/O Protection

Frontgrade UT54LVDS328 400 Mbps Octal LVDS Repeater Device Features

- Data rates up to 400.0 Mbps per channel / 200 MHz clock channel
- 3.3V power supply / 3.5mA LVDS TX output drive current / Total integrated dose (TID): 1Mrad(Si)
- Extends SpW channel reach - x1 UT54LVDS328 octal LVDS repeater supports x2 SpW ports
- Protects Versal™ FPGA LVDS I/Os: General High-Speed Serial LVDS, ADC JESD204, and SpW Interfaces
- Cold sparing all pins / 48-lead CFP package

Frontgrade UT54LVDS454 1.25 Gbps Dual, Full-Duplex / Quad, Simplex LVDS Repeater Device Features

- Data rates up to 1.25 Gbps per channel / protocol independent
- 2.5V power supply / Selectable 3.5mA or 7.0mA TX output drive currents / Total integrated dose (TID): 100krad(Si)
- Extends SpW channel reach - x1 UT54LVDS454 quad LVDS repeater supports x1 SpW port
- Protects Versal™ FPGA LVDS I/Os: General High-Speed Serial LVDS, ADC JESD204, and SpW Interfaces
- Cold sparing all pins / 71-land C-CGA/C-LGA package

AMD Versal™ FPGA to LVDS Repeater Design Considerations

- SpW Interfacing: SpW IP Cores are Available for the Versal™ FPGA
- https://www.xilinx.com/products/intellectual-property/1-12nthtb.html / https://soc-e.com/spacewire-ip-core/
- Frontgrade LVDS Repeaters Support SpW Interfacing to the Versal™ FPGA once the Versal I/Os are Configured as a SpW Port or Ports
- Frontgrade LVDS Repeaters Also Protect Versal™ FPGA LVDS I/Os: General High-Speed Serial LVDS, ADC JESD204, and SpW Interfaces

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THANK YOU